

Description

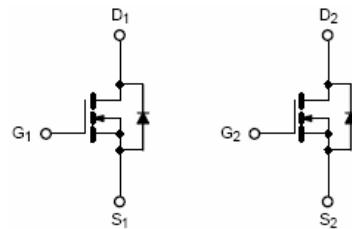
The LCE9926 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

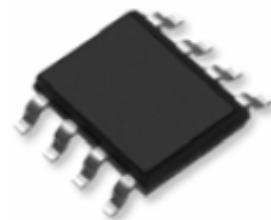
- $V_{DS} = 20V, I_D = 6A$
- $R_{DS(ON)} < 28m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} < 37m\Omega @ V_{GS}=2.5V$
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
9926	LCE9926	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain Current-Continuous	I_D	6	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D (100^\circ C)$	3.8	A
Pulsed Drain Current	I_{DM}	25	A
Maximum Power Dissipation	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	100	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

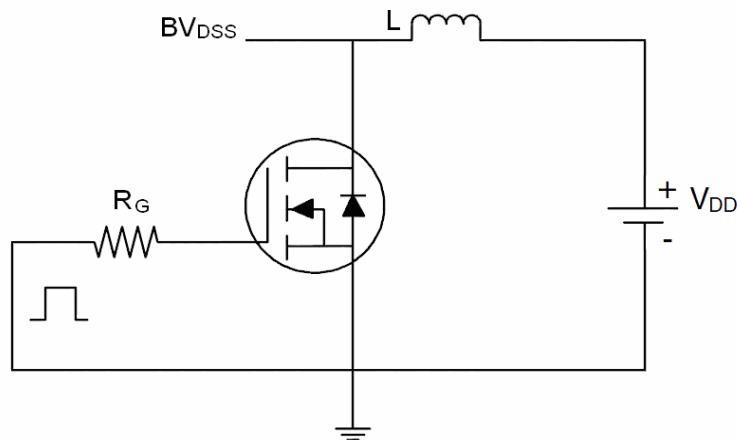
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20	22	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 10\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.5	0.7	1.2	V
Drain-Source On-State Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=6\text{A}$	-	20	28	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=5\text{A}$	-	26	37	
Forward Transconductance	g_{FS}	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=6\text{A}$	20	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=10\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	640	-	PF
Output Capacitance	C_{oss}		-	140	-	PF
Reverse Transfer Capacitance	C_{rss}		-	80	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=10\text{V}, I_{\text{D}}=1\text{A}$ $V_{\text{GEN}}=4.5\text{V}, R_{\text{G}}=6\Omega$	-	8	-	nS
Turn-on Rise Time	t_{r}		-	9	-	nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	15	-	nS
Turn-Off Fall Time	t_{f}		-	4	-	nS
Total Gate Charge	Q_{g}	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=3\text{A}, V_{\text{GS}}=4.5\text{V}$	-	10	-	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	nC
Gate-Drain Charge	Q_{gd}		-	1.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=1.7\text{A}$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_{S}		-	-	6	A

Notes:

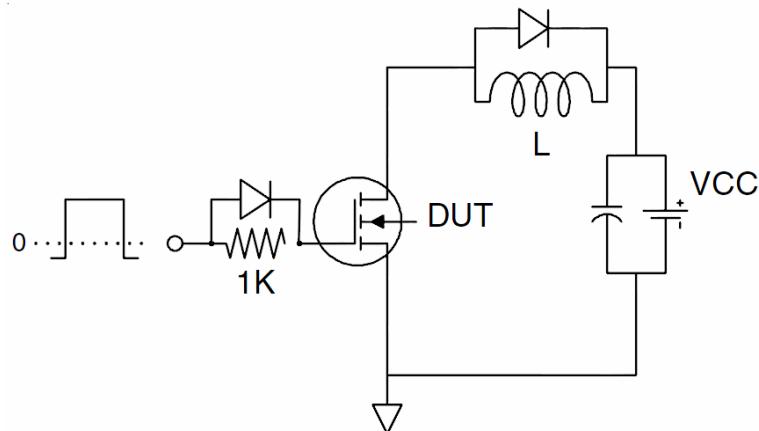
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

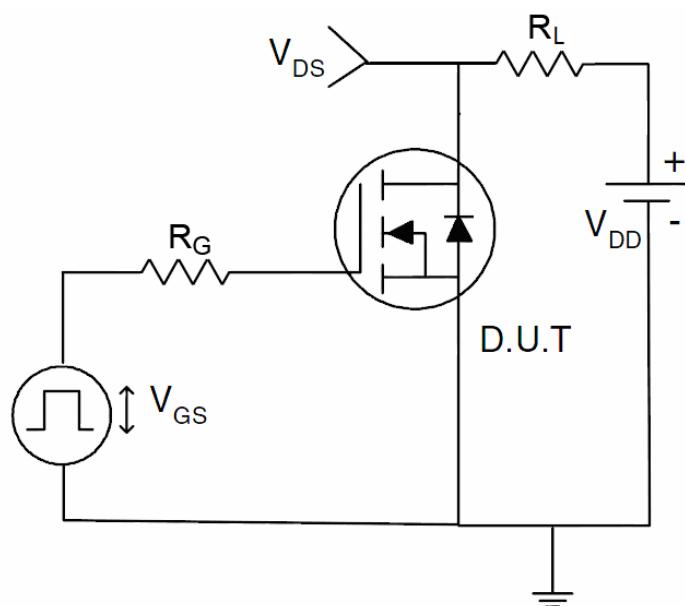
1) E_{AS} Test Circuits



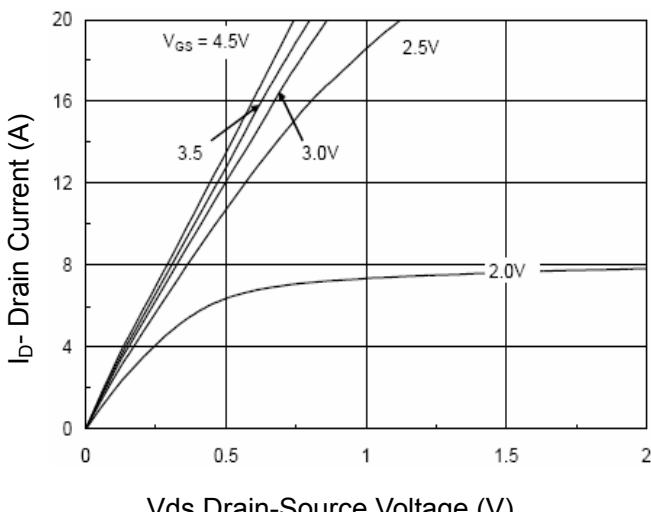
2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:

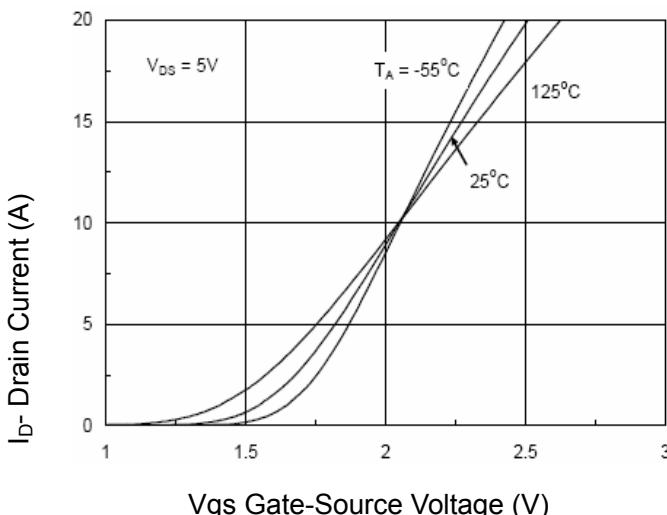


Typical Electrical and Thermal Characteristics (Curves)



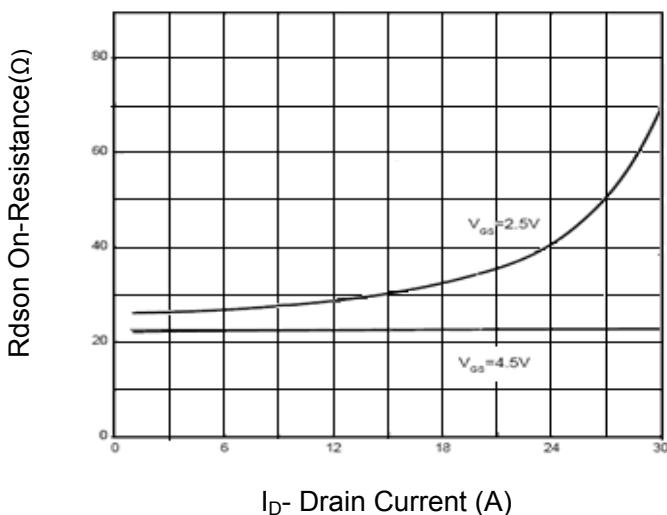
V_{DS} Drain-Source Voltage (V)

Figure 1 Output Characteristics



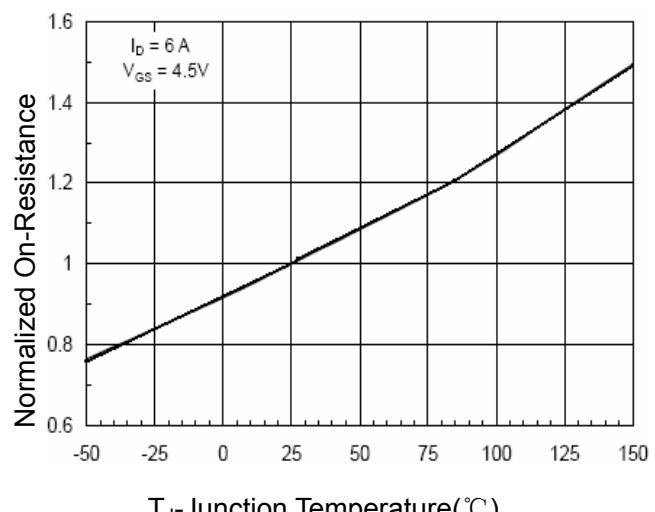
V_{GS} Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



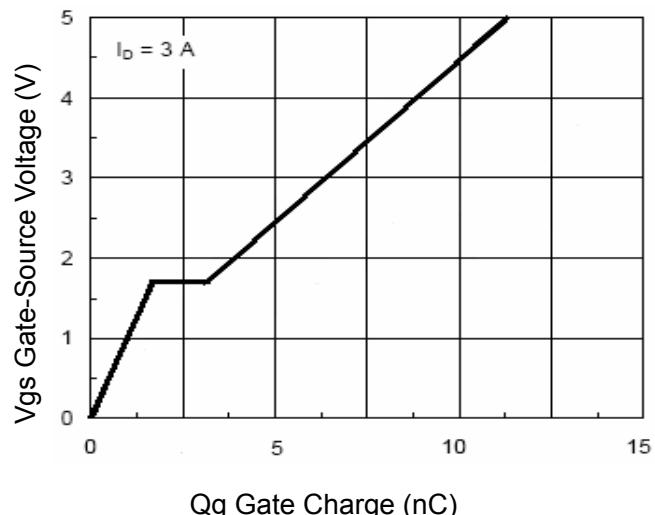
I_D Drain Current (A)

Figure 3 Rdson- Drain Current



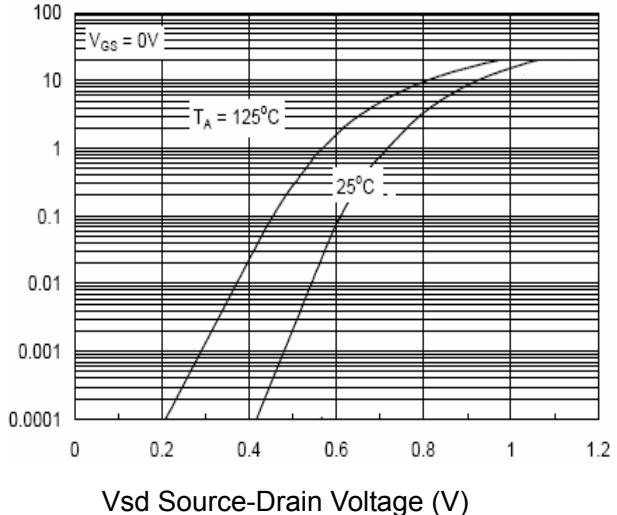
T_J -Junction Temperature(°C)

Figure 4 Rdson-JunctionTemperature



Q_G Gate Charge (nC)

Figure 5 Gate Charge



V_{SD} Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

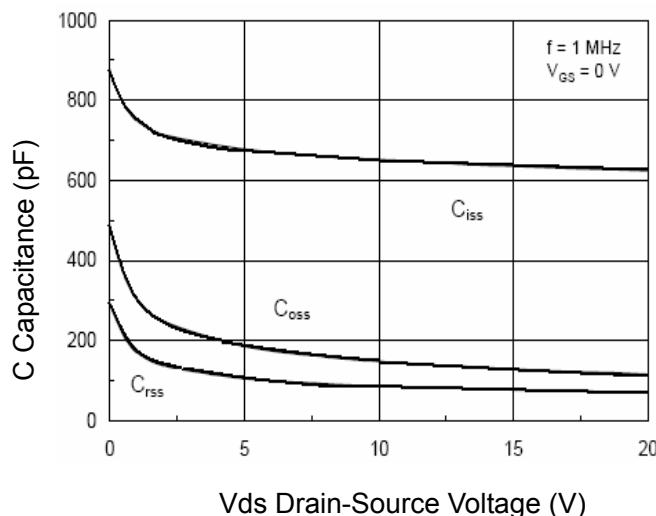


Figure 7 Capacitance vs Vds

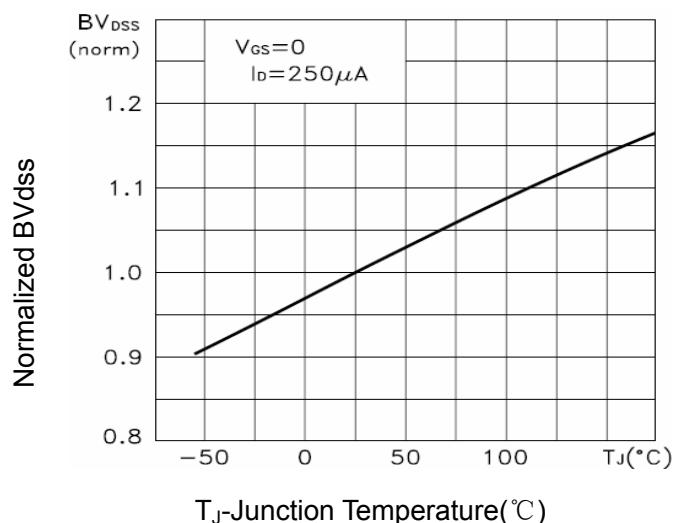


Figure 9 BV_{dss} vs Junction Temperature

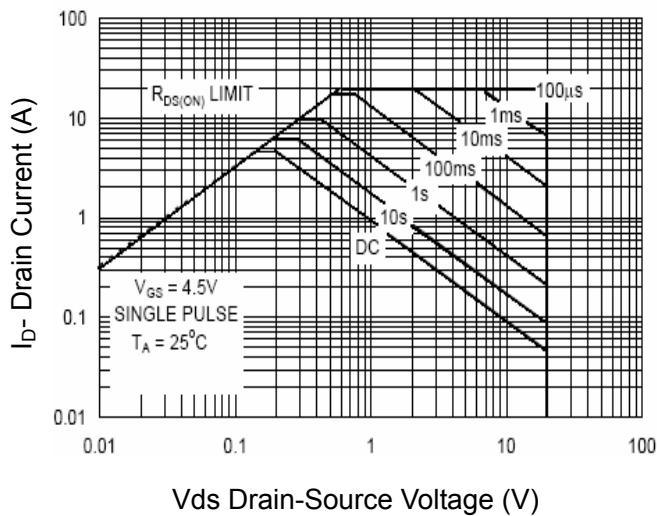


Figure 8 Safe Operation Area

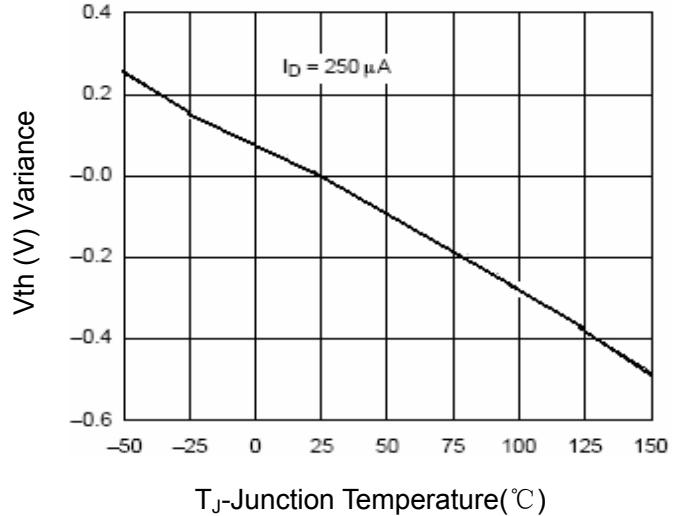


Figure 10 $V_{GS(th)}$ vs Junction Temperature

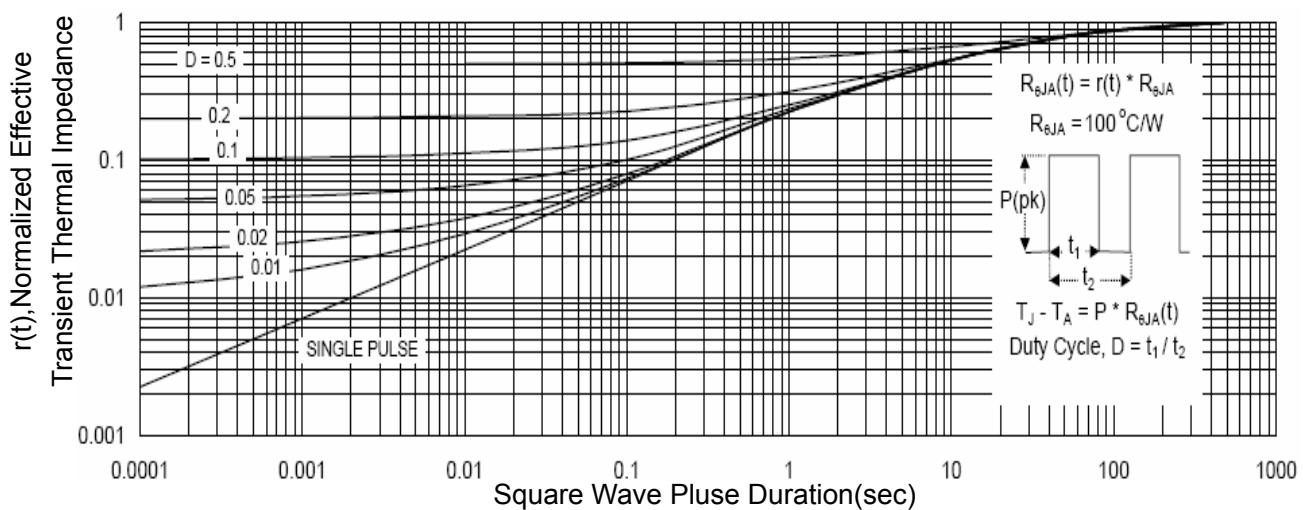
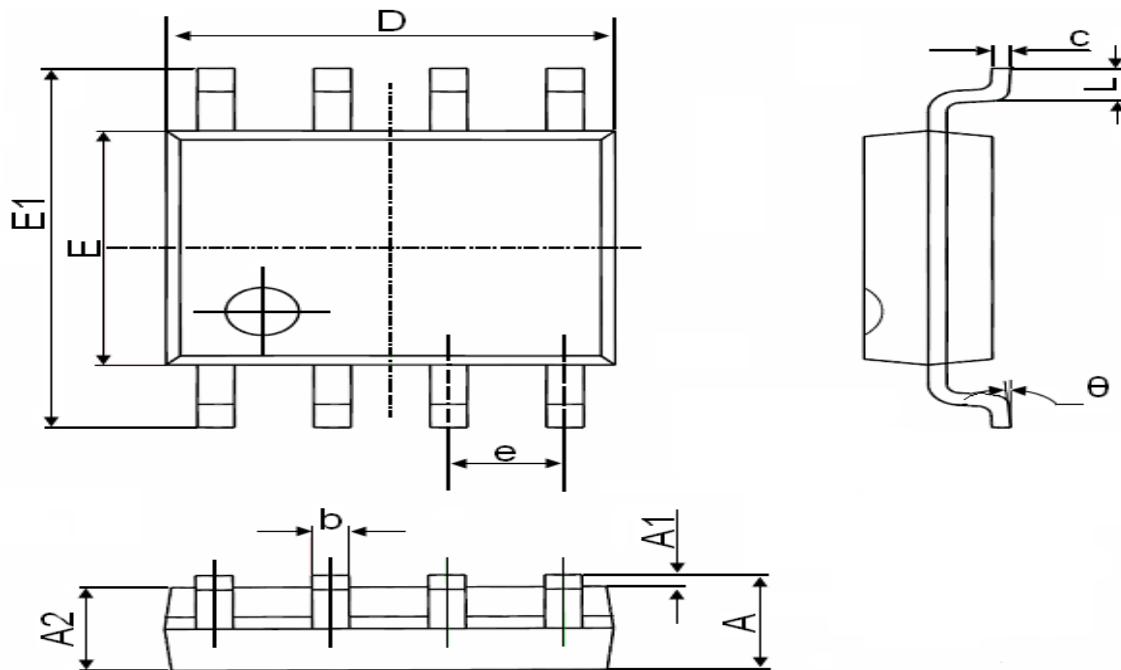


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°		8°	

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