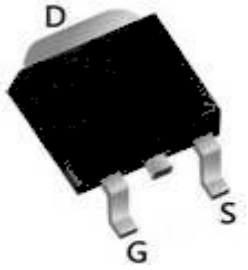
LMAK13P20

-200V P-Channel Enhancement Mode MOSFET

Description

The LMAK13P20 is silicon P-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

Dimensions TO-252

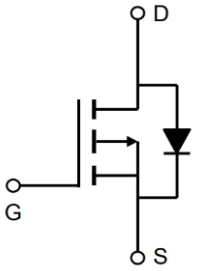


General Features

VDS =-200V,ID =-13A

RDS(ON) <0.42Ω@ VGS=10V

Pin Configuration



Application

- Power amplifier
- Motor drive

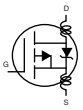
Package Marking and Ordering Information

Device	Device Marking	Device Package	Reel Size	Tape width	Quantity
LMAK13P20	AP13P20D	TO-252	-	-	2500 units

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-200	V
VGS	Gate-Source Voltage	± 20	V
ID T_C = 25 °C	Continuous Drain Current	-13	A
ID T_C = 100 °C	Continuous Drain Current	-7.2	A
IDM	Pulsed Drain Current [a]	-52	A
EAS	Single Pulse Avalanche Energy [b]	750	mJ
IAR	Repetitive Avalanche Current [a]	-11	A
EAR	Repetitive Avalanche Energy [a]	13	mJ
P_D T_C = 25 °C	Maximum Power Dissipation	125	W
dV/dt	Peak Diode Recovery dV/dt [c]	-5.0	V/ns
TJ, Tstg	Operating Junction and Storage Temperature Range	-55 to +150	°C
RthJA	Maximum Junction-to-Ambient	62	°C/W
RthCS	Case-to-Sink, Flat, Greased Surface	0.50	°C/W
RthJC	Maximum Junction-to-Case (Drain)	1.0	°C/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-200	-	-	V
□V_{DS}/T_J	V_{DS} Temperature Coefficient	Reference to 25 °C, I_D = -1 mA	-	-0.2	-	V/°C
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-2.0	-	-4.0	V
I_{GSS}	Gate-Source Leakage	V_{GS} = ± 20 V	-	-	± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -200 V, V_{GS} = 0 V	-	-	-100	μA
I_{DSS}		V_{DS} = -160 V, V_{GS} = 0 V, T_J = 125 °C	-	-	-500	
$R_{DS(on)}$	Drain-Source On-State Resistance	V_{GS} = -10 V I_D = -5.5 A [b]	-	0.34	0.42	Ω
g_{fs}	Forward Transconductance	V_{DS} = -50 V, I_D = -6.6 A [b]	4.1	-	-	S
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 5	-	1200	-	pF
C_{oss}	Output Capacitance		-	370	-	
C_{rss}	Reverse Transfer Capacitance		-	81	-	
Q_g	Total Gate Charge	V_{GS} = -10 V; I_D = -11 A, V_{DS} = -160 V, see fig. 6 and 13 [b]	-	-	44	nC
Q_{gs}	Gate-Source Charge		-	-	7.1	
Q_{gd}	Gate-Drain Charge		-	-	27	
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -100 V, I_D = -11 A, R_g = 9.1 Ω, R_D = 8.6 Ω, see fig. 10 [b]	-	14	-	ns
t_r	Rise Time		-	43	-	
$t_{d(off)}$	Turn-Off Delay Time		-	39	-	
t_f	Fall Time		-	38	-	
R_g	Gate Input Resistance	f = 1 MHz, open drain	0.3	-	1.7	Ω
I_S	Continuous Source-Drain Diode Current	Between lead, 6 mm (0.25") from package and center of die contact 	-	-	-11	A
I_{SM}	Pulsed Diode Forward Current [a]		-	-	-44	
V_{SD}	Body Diode Voltage	T_J = 25 °C, I_S = -11 A, V_{GS} = 0 V [b]	-	-	-5	V
t_{rr}	Body Diode Reverse Recovery Time	T_J = 25 °C, I_F = -11 A, dI/dt = 100 A/μs [b]	-	250	300	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	2.9	3.6	μC
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

Typical Electrical and Thermal Characteristics

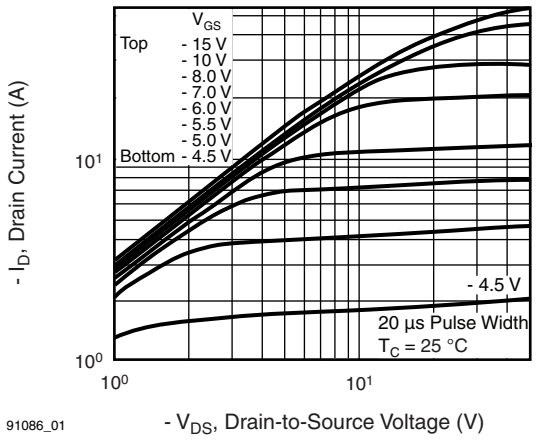


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

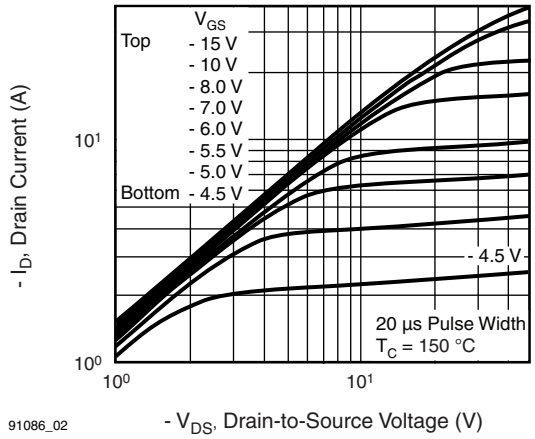


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

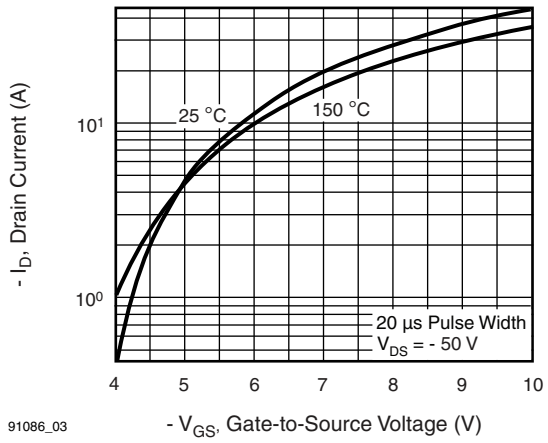


Fig. 3 - Typical Transfer Characteristics

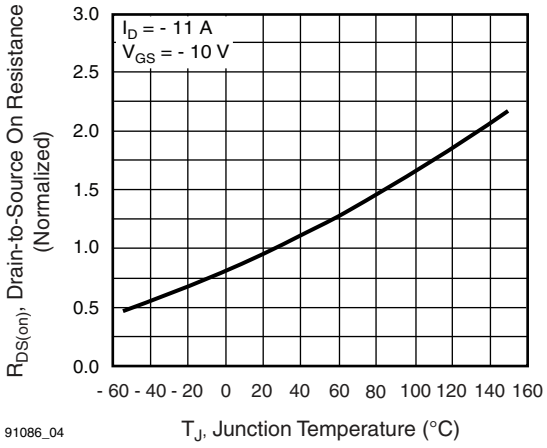


Fig. 4 - Normalized On-Resistance vs. Temperature

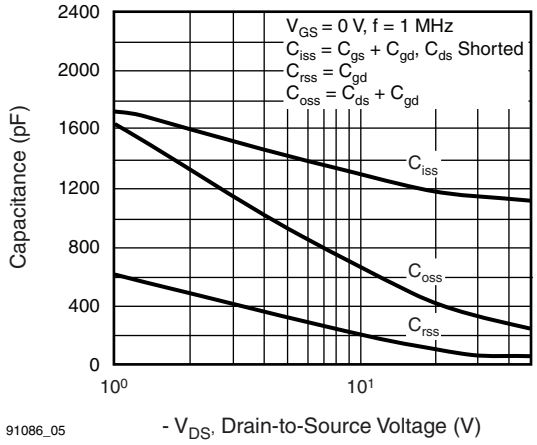


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

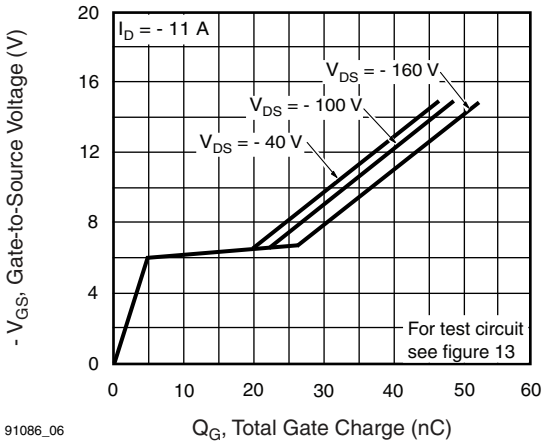


Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage

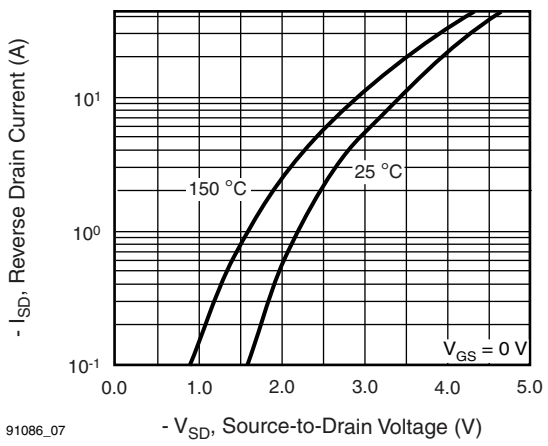


Fig. 7 - Typical Source-Drain Diode Forward Voltage

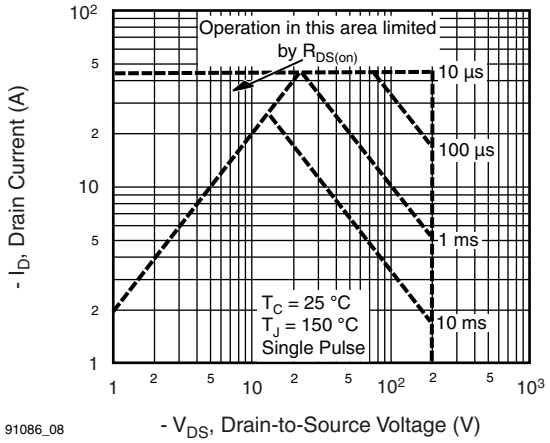


Fig. 8 - Maximum Safe Operating Area

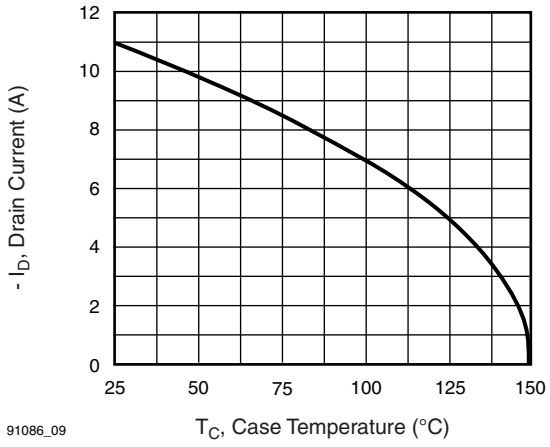


Fig. 9 - Maximum Drain Current vs. Case Temperature

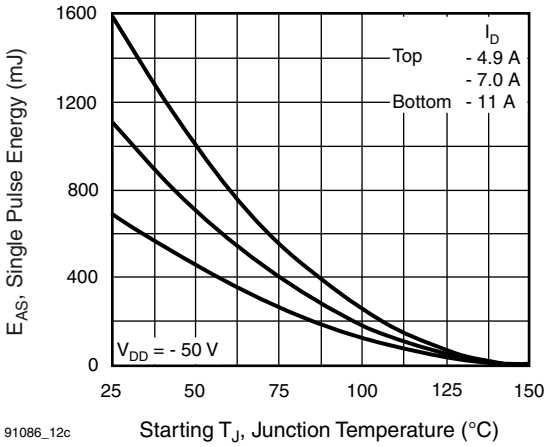


Fig. 10 - Maximum Avalanche Energy vs. Drain Current

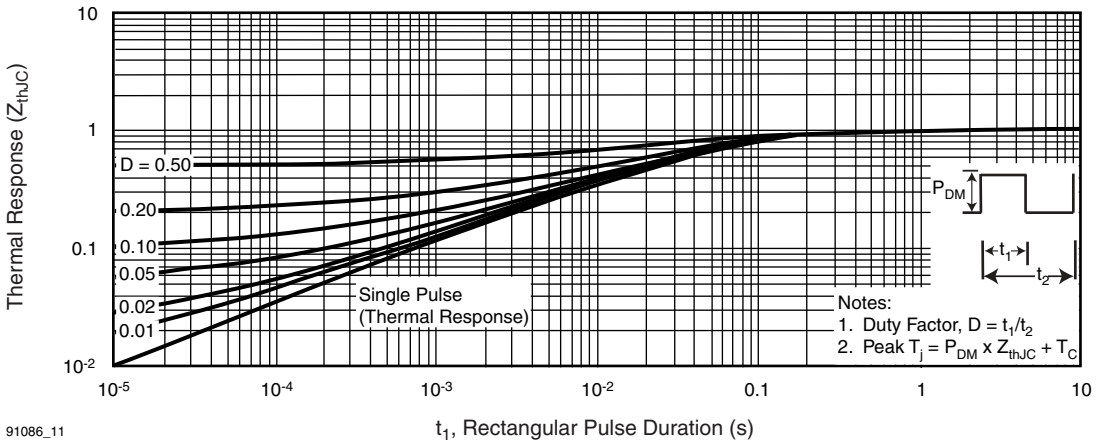
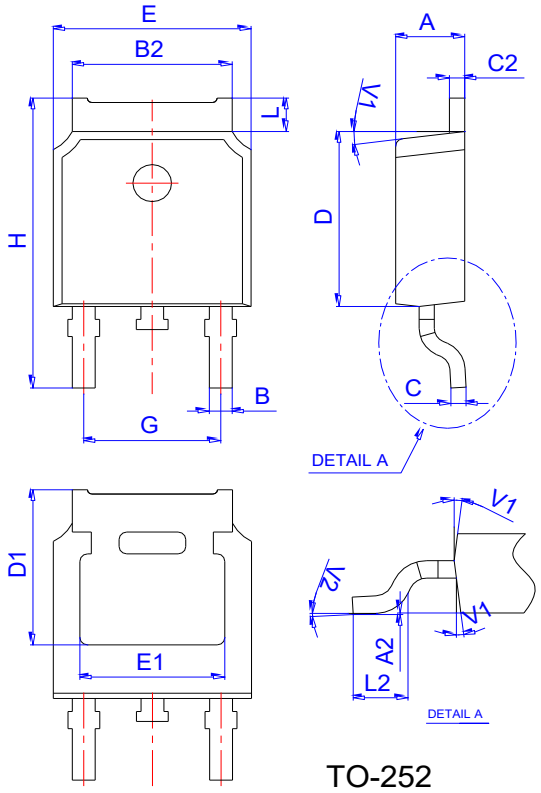


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

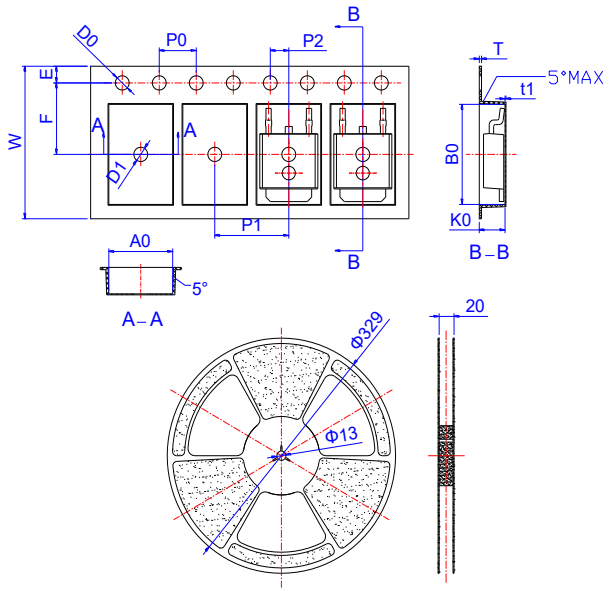
Package Mechanical Data



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

Shanghai Leiditech Electronic Co.,Ltd
Email: sale1@leiditech.com
Tel : +86- 021 50828806
Fax : +86- 021 50477059