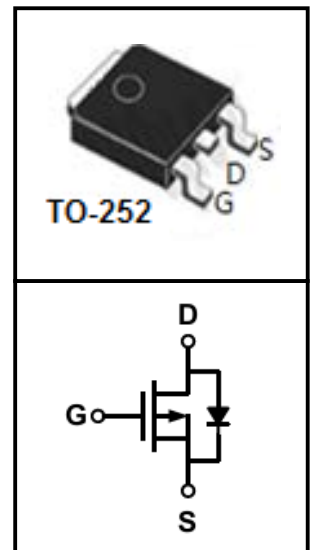


**FEATURES**

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

**APPLICATIONS**

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

**Device Marking and Package Information**

Device	Package	Marking
LMD10P100	TO-252	

**Absolute Maximum Ratings at  $T_j = 25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Value	Unit
Drain-Source Voltage ( $V_{GS} = 0V$ )	$V_{DSS}$	-100	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1)	$I_D$	-30	A
Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1)		-21	A
Pulsed Drain Current (note2)	$I_{DM}$	-52	A
Gate Source Voltage	$V_{GSS}$	$\pm 20$	V
Single Pulse Avalanche Energy (note3)	$E_{AS}$	110	mJ
Power Dissipation $T_C = 25^\circ\text{C}$ (note4)	$P_D$	69.3	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55~+150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-Case (note1)	$R_{\theta JC}$	1.3	K/W
Thermal Resistance, Junction-to-Ambient (note1)	$R_{\theta JA}$	62	

Electrical Characteristics $T_j = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	-100	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	-50	$\mu A$
		$V_{DS} = -100V, V_{GS} = 0V, T_J = 55^\circ\text{C}$	--	--	-60	$\mu A$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	-1.2	--	-2.5	V
Drain-Source On-Resistance (note2)	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -12A$	--	80	100	$m\Omega$
		$V_{GS} = -4.5V, I_D = -9A$	--	88	115	$m\Omega$
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = -20V,$ $f = 1.0\text{MHz}$	--	3029	--	pF
Output Capacitance	$C_{oss}$		--	129	--	
Reverse Transfer Capacitance	$C_{rss}$		--	76	--	
Total Gate Charge (4.5V)	$Q_g$	$V_{DS} = -50V, I_D = -20A,$ $V_{GS} = -10V$	--	44.5	--	nC
Gate-Source Charge	$Q_{gs}$		--	9.13	--	
Gate-Drain Charge	$Q_{gd}$		--	5.93	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = -50V, I_D = -10A,$ $V_{GS} = -10V, R_G = 3.3\Omega$	--	12	--	ns
Turn-on Rise Time	$t_r$		--	27.4	--	
Turn-off Delay Time	$t_{d(off)}$		--	79	--	
Turn-off Fall Time	$t_f$		--	53.6	--	
<b>Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	-30	A
Pulsed Diode Forward Current	$I_{SM}$		--	--	-52	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = -1A, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = -14A$ $di_F/dt = 100A/\mu s$	--	38.7	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	22.4	--	nC

**Notes**

1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$  , duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is  $V_{DD} = 25V, V_{GS} = 10V, L = 0.85mH$
4. The power dissipation is limited by  $175^\circ\text{C}$  junction temperature
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

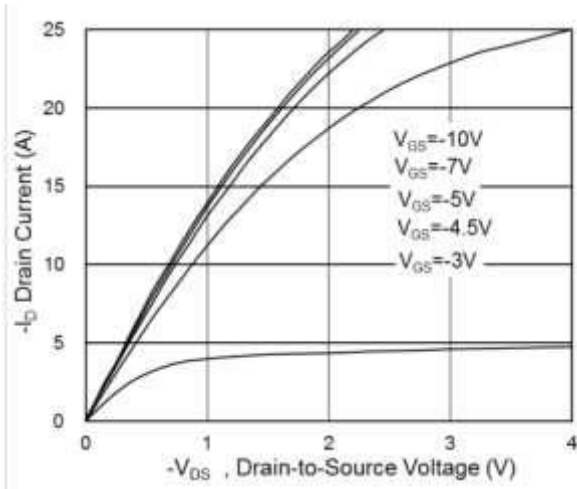


Fig.1 Typical Output Characteristics

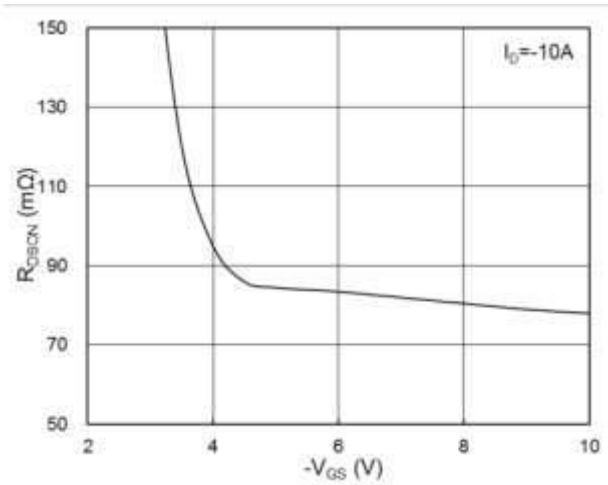


Fig.2 On-Resistance vs. G-S Voltage

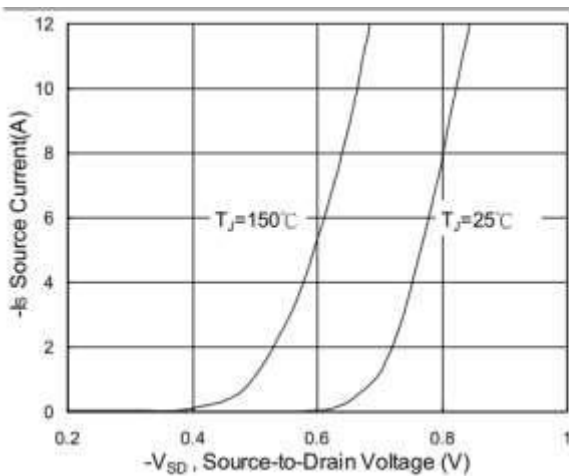


Fig.3 Forward Characteristics of Reverse Diode

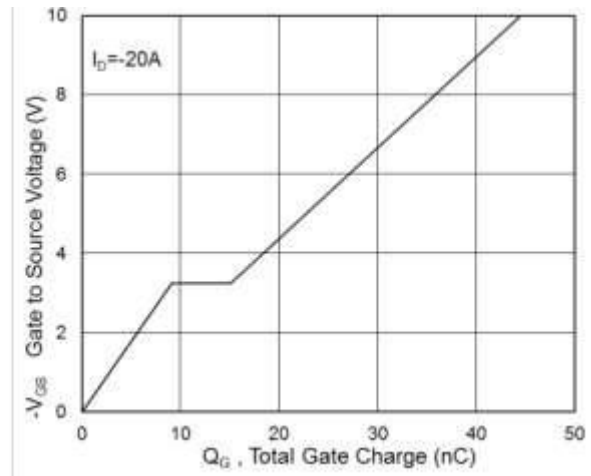


Fig.4 Gate-Charge Characteristics

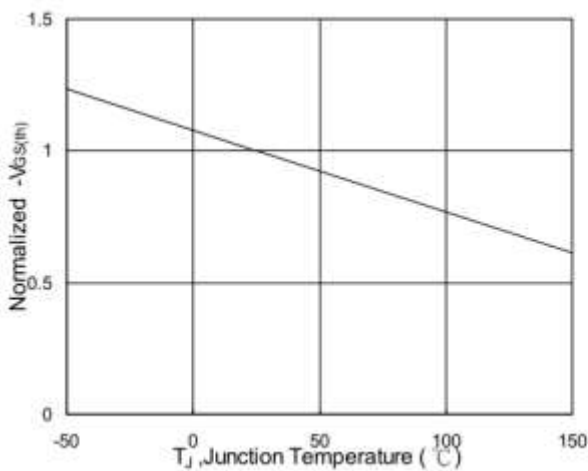


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

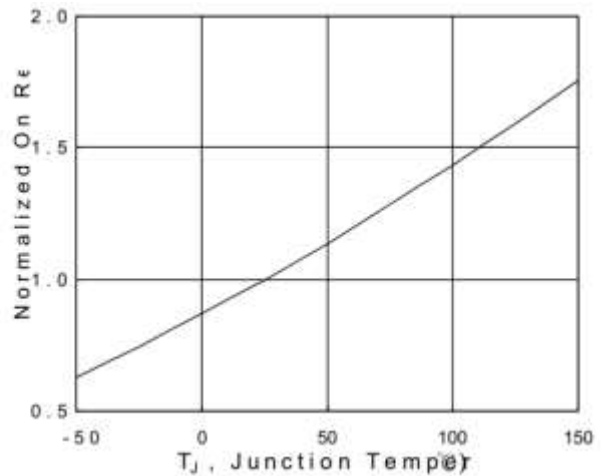


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

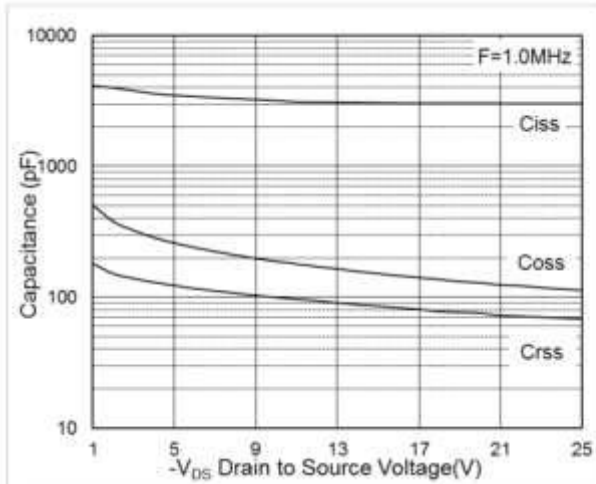


Fig.7 Capacitance

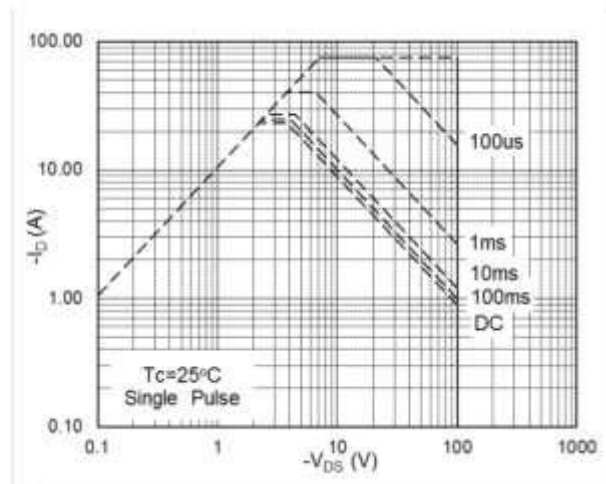


Fig.8 Safe Operating Area

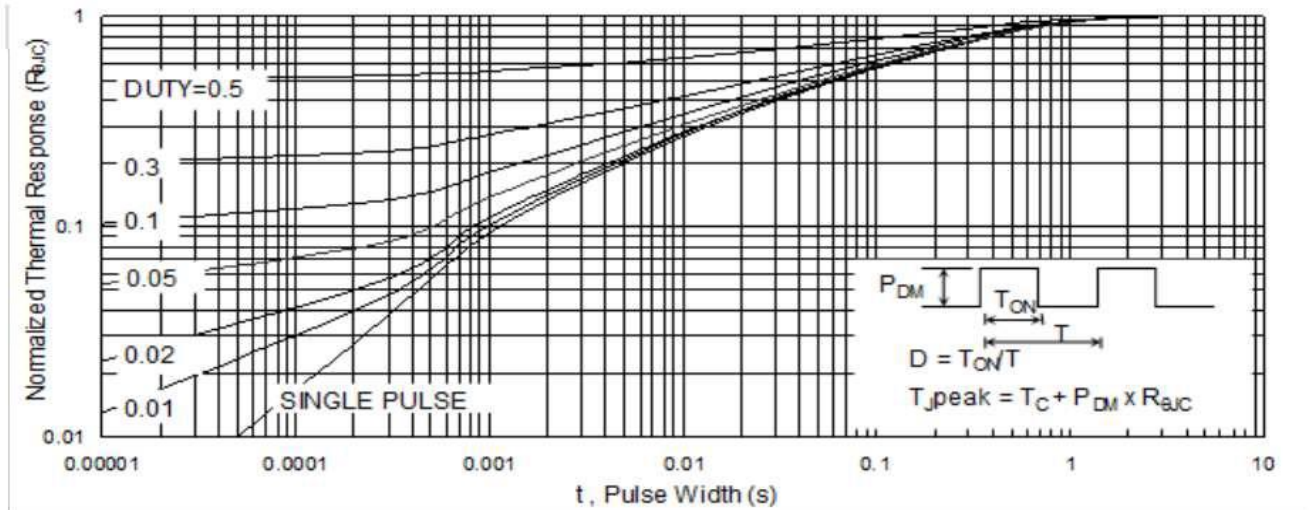
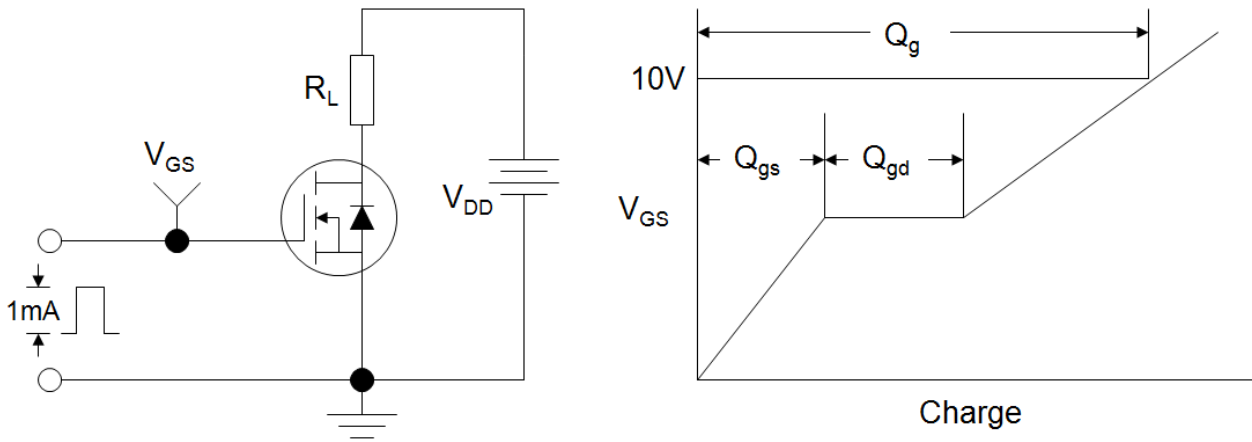
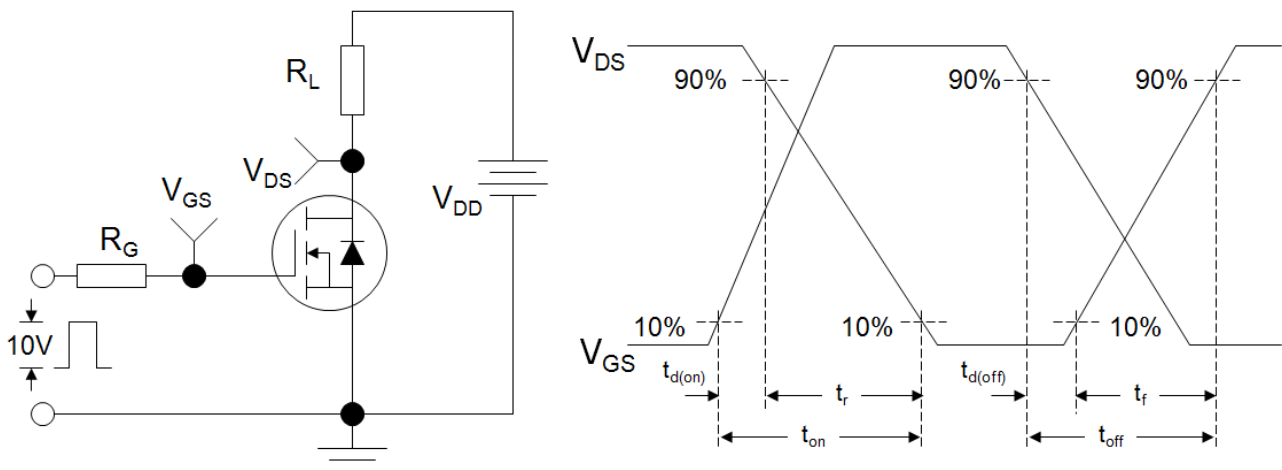


Fig.9 Normalized Maximum Transient Thermal Impedance

**Figure A: Gate Charge Test Circuit and Waveform**



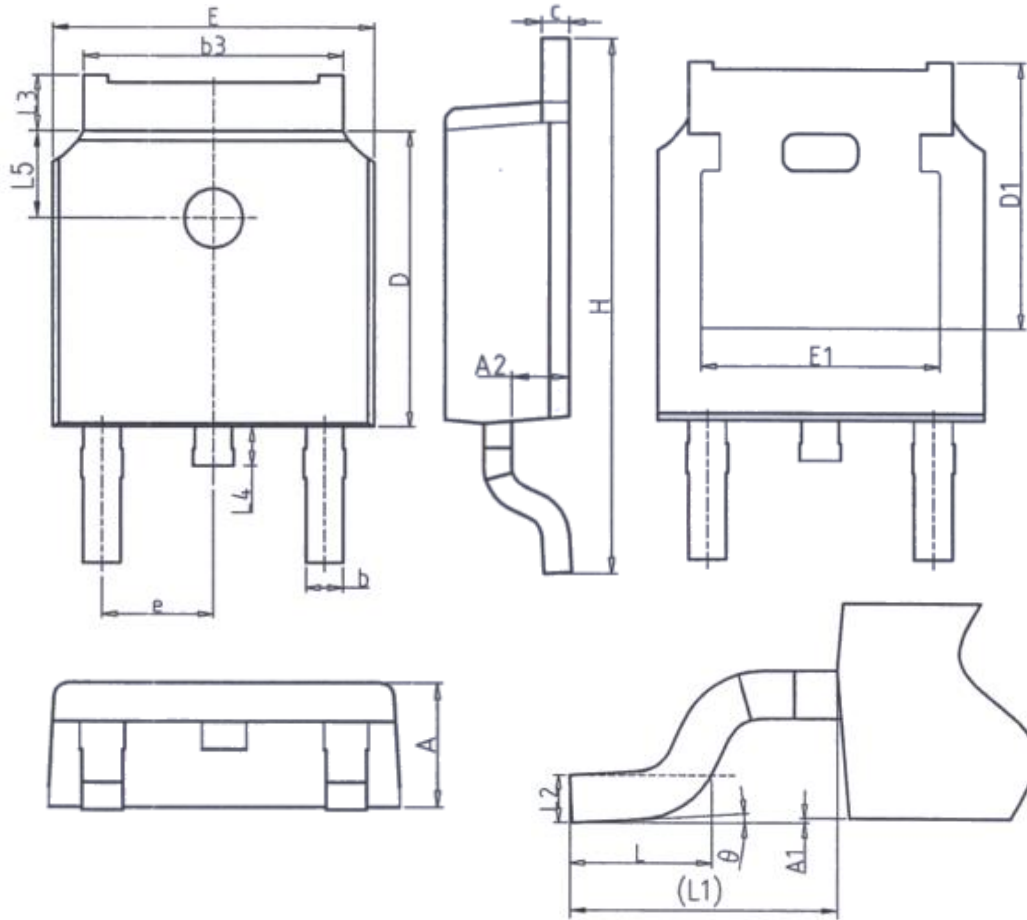
**Figure B: Resistive Switching Test Circuit and Waveform**



**Figure C: Unclamped Inductive Switching Test Circuit and Waveform**



## TO252 PACKAGE INFORMATION



Unit: mm		
Symbol	Min.	Max.
A	2.20	2.40
A1	0.00	0.20
A2	0.97	1.17
b	0.68	0.90
b3	5.20	5.50
c	0.43	0.63
D	5.98	6.22
D1	5.30REF	
E	6.40	6.80
E1	4.63	-

Unit: mm		
Symbol	Min.	Max.
e	2.286BSC	
H	9.40	10.50
L	1.38	1.75
L1	2.90REF	
L2	0.51BSC	
L3	0.88	1.28
L4	-	1.00
L5	1.65	1.95
$\theta$	0°	8°