Leiditech

LM10185

P-Channel Enhancement Mode Power MOSFET

General Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	-100V
I_D (at V_{GS}=-10V)	-15A
$R_{DS(ON)}$ (at V_{GS}=-10V)	160mΩ(Typ)

100% UIS TESTED!
100% ΔVds TESTED!

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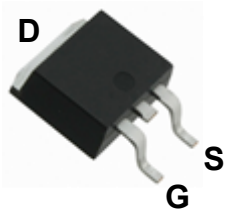
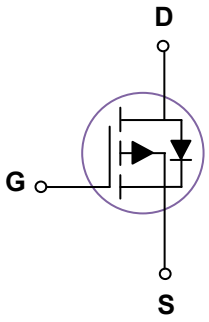




Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	TC=25°C	I_D	-15	A
	TC=100°C	I_D	-9.5	A
Single pulse avalanche energy		E_{AS}	30	mJ
Maximum Power Dissipation		P_D	50	W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		1.4	℃ /W
Thermal Resistance unction-to-Ambient	$R_{\theta JA}$		60	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=-250μA	-100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-100V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-1.0		-3.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=-10V, I_D=-5A		160	200	mΩ
		V_{GS}=-4.5V, I_D=-2A		180	220	mΩ
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{DS}=-25V,V_{GS}=0V , F=1.0MHz		1419		pF
C_{oss}	Output Capacitance			89		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-50V,I_D=-5A , V_{GS}=-10V, R_G=25Ω		18		nS
t_r	Turn-on Rise Time			8		nS
$t_{d(off)}$	Turn-Off Delay Time			100		nS
t_f	Turn-Off Fall Time			30		nS
Q_g	Total Gate Charge	V_{DS}=-80V,I_D=-5A , V_{GS}=-10V		20		nC
Q_{gs}	Gate-Source Charge			3.5		nC
Q_{gd}	Gate-Drain Charge			4.6		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=-1A		0.72	1.4	V

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=22A.,Starting T_J=25℃
3. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
4. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

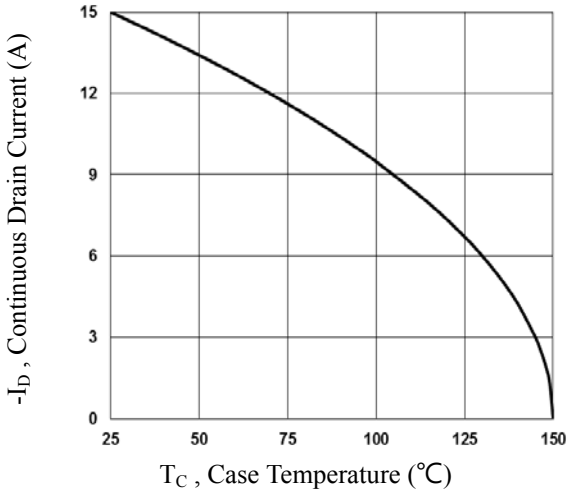


Fig.1 Continuous Drain Current vs. T_C

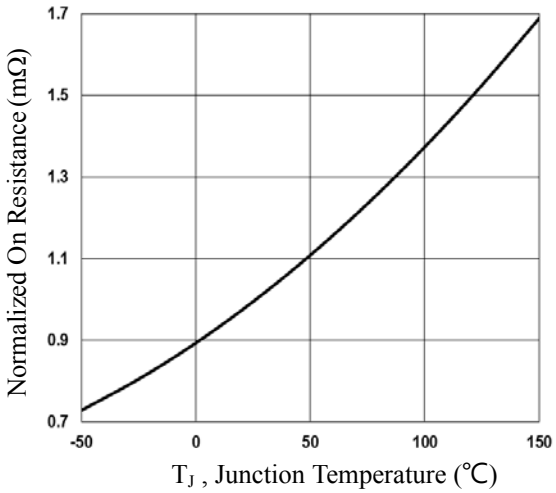


Fig.2 Normalized RDSON vs. T_J

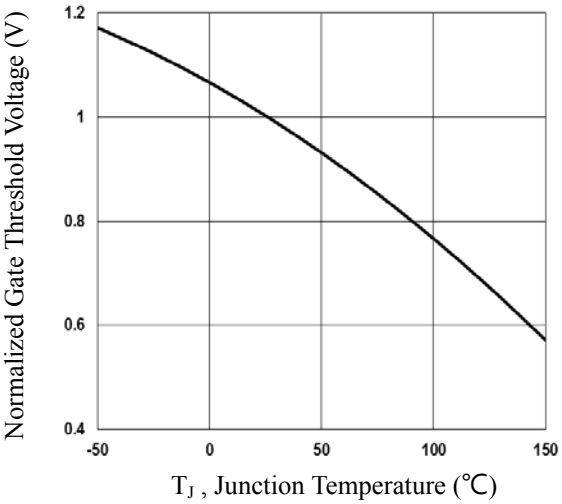


Fig.3 Normalized V_{th} vs. T_J

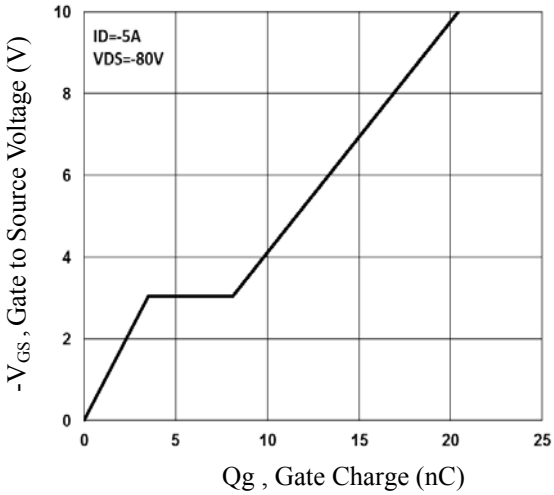


Fig.4 Gate Charge Waveform

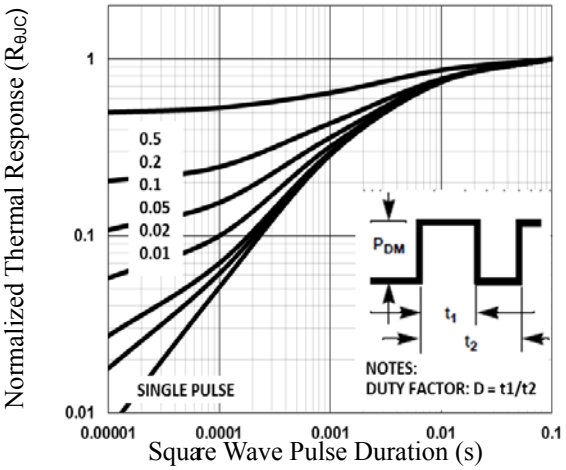


Fig.5 Normalized Transient Impedance

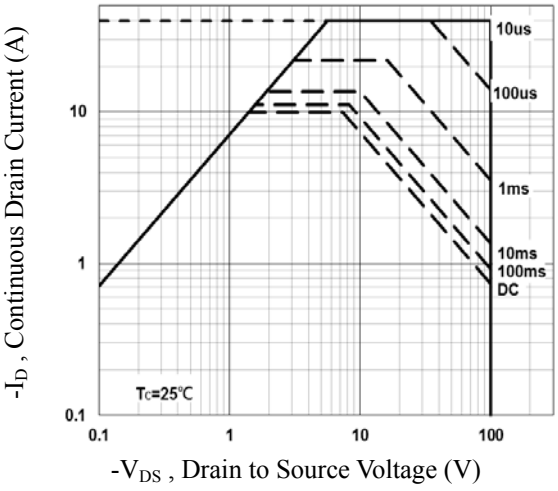


Fig.6 Maximum Safe Operation Area

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

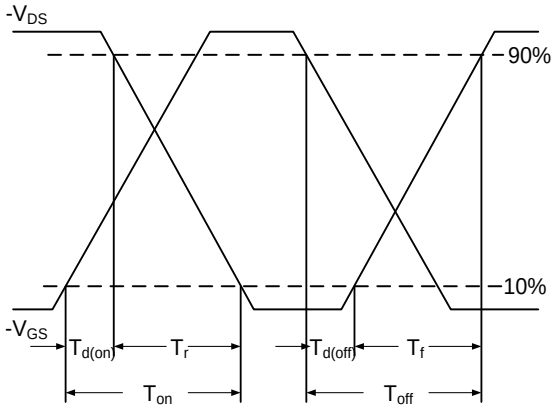


Fig.7 Switching Time Waveform

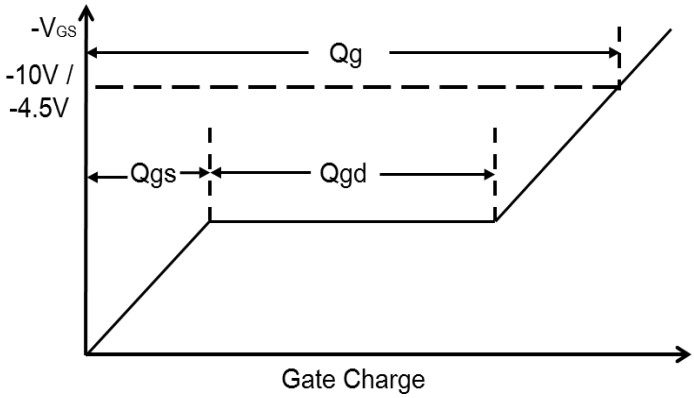
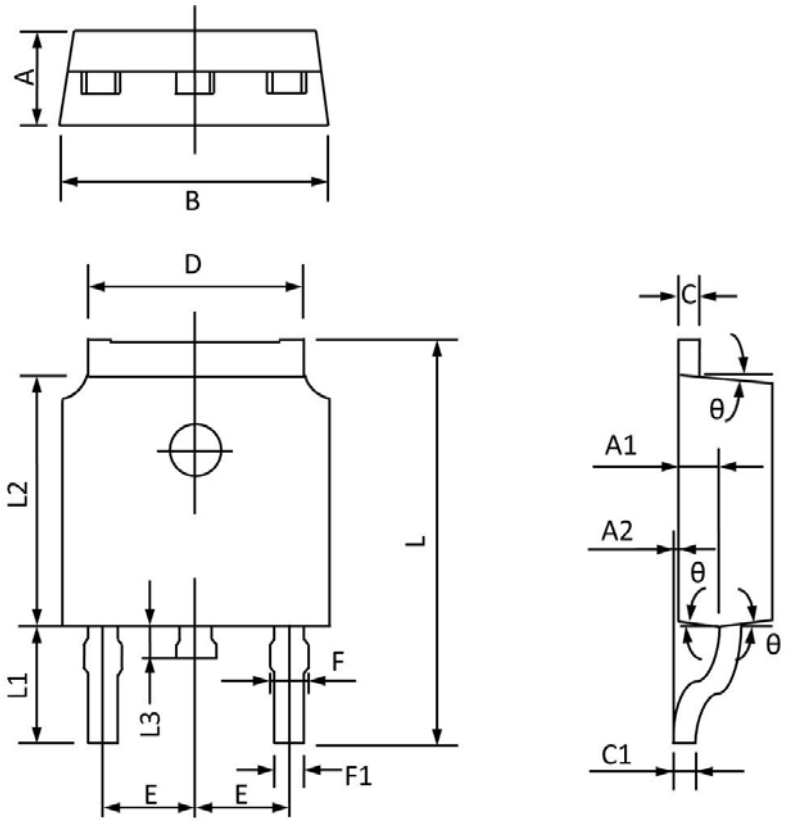


Fig.8 Gate Charge Waveform

TO252 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.20	2.40	0.087	0.094
A1	0.91	1.11	0.036	0.044
A2	0.00	0.15	0.000	0.006
B	6.50	6.70	0.256	0.264
C	0.46	0.580	0.018	0.230
C1	0.46	0.580	0.018	0.030
D	5.10	5.46	0.201	0.215
E	2.186	2.386	0.086	0.094
F	0.74	0.94	0.029	0.037
F1	0.660	0.860	0.026	0.034
L	9.80	10.40	0.386	0.409
L1	2.9REF		0.114REF	
L2	6.00	6.20	0.236	0.244
L3	0.60	1.00	0.024	0.039
θ	3°	9°	3°	9°

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