

FEATURES

- TrenchFET® Power MOSFET: 1.8-V Rated
- Gate-Source ESD Protected
- High-Side Switching
- Low On-Resistance: 0.4 Ω
- Low Threshold: 0.8 V (typ)
- Fast Switching Speed: 10 ns
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

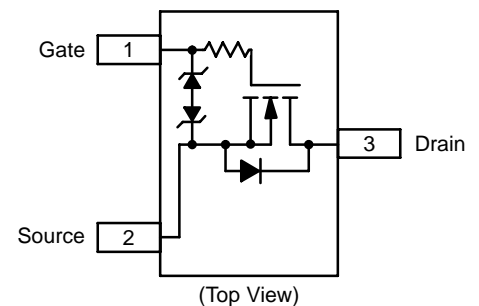
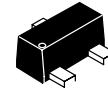
BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

Dimensions SOT-523



ORDERING INFORMATION

Device	Marking	Shipping
LM4153	A	3000/Tape&Reel

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	20		V	
Gate-Source Voltage	V_{GS}	± 10			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^b	I_D	$T_A = 25^\circ\text{C}$	700	600	mA
		$T_A = 85^\circ\text{C}$	400	350	
Pulsed Drain Current ^a	I_{DM}	1000			
Continuous Source Current (diode conduction) ^b	I_S	275	250		
Maximum Power Dissipation ^b for SC-75	P_D	$T_A = 25^\circ\text{C}$	175	150	mW
		$T_A = 85^\circ\text{C}$	90	80	
Maximum Power Dissipation ^b for SC-89	P_D	$T_A = 25^\circ\text{C}$	275	250	
		$T_A = 85^\circ\text{C}$	160	140	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

Notes

- d. Pulse width limited by maximum junction temperature.
- e. Surface Mounted on FR4 Board.



SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.3		1	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85^\circ\text{C}$			5	μA
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	700			mA
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 500\ \text{mA}$		0.25	0.4	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 200\ \text{mA}$		0.35	0.6	
		$V_{GS} = 1.8\ \text{V}, I_D = 100\ \text{mA}$		0.65	0.8	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}, I_D = 400\ \text{mA}$		1.0		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 150\ \text{mA}, V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 250\ \text{mA}$		750		pC
Gate-Source Charge	Q_{gs}			75		
Gate-Drain Charge	Q_{gd}			225		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 47\ \Omega$ $I_D \cong 200\ \text{mA}, V_{GEN} = 4.5\ \text{V}, R_G = 10\ \Omega$		5		ns
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			25		
Fall Time	t_f			11		

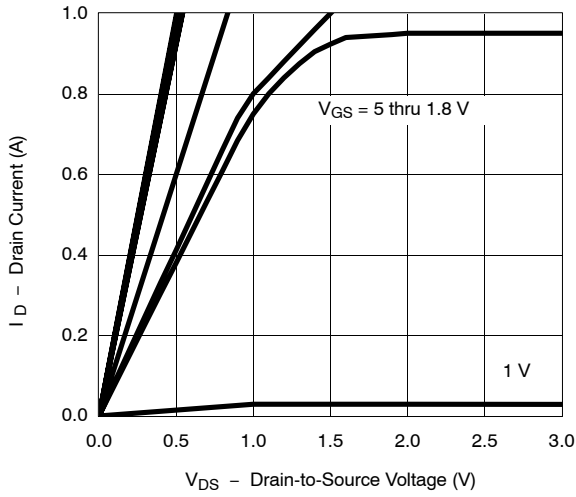
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

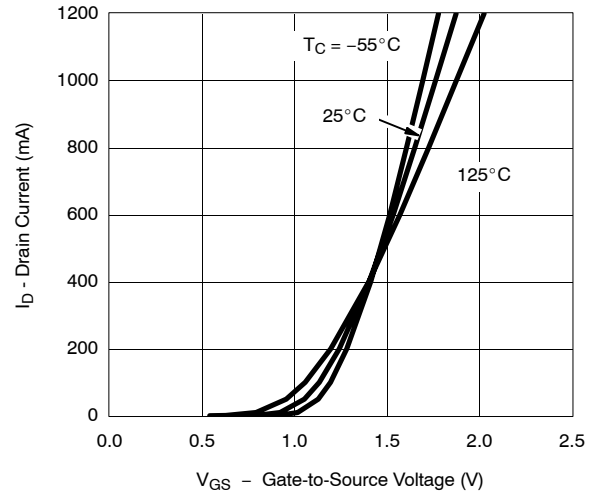
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS NOTED)

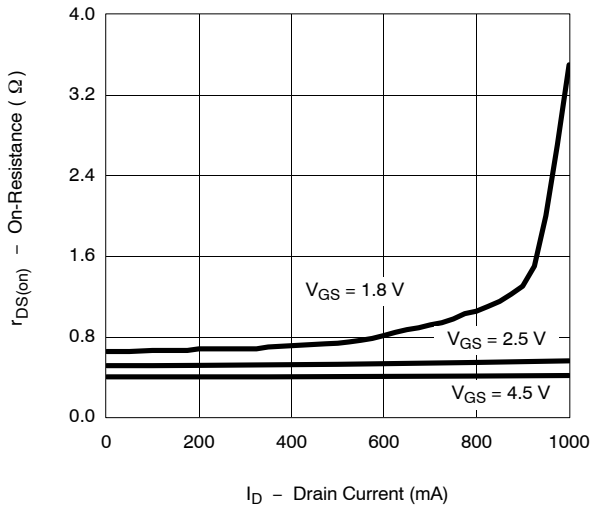
Output Characteristics



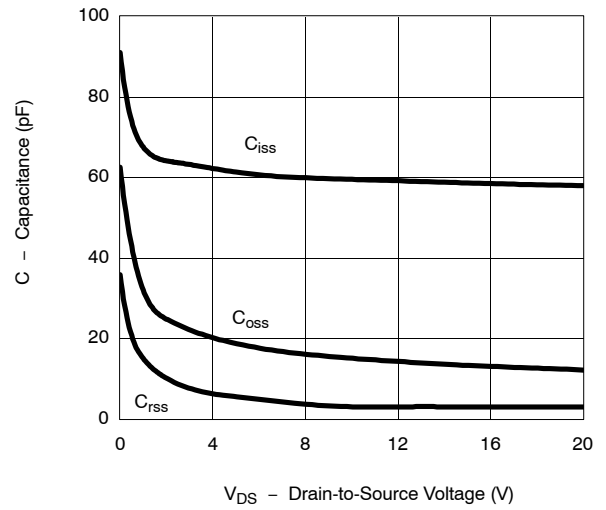
Transfer Characteristics



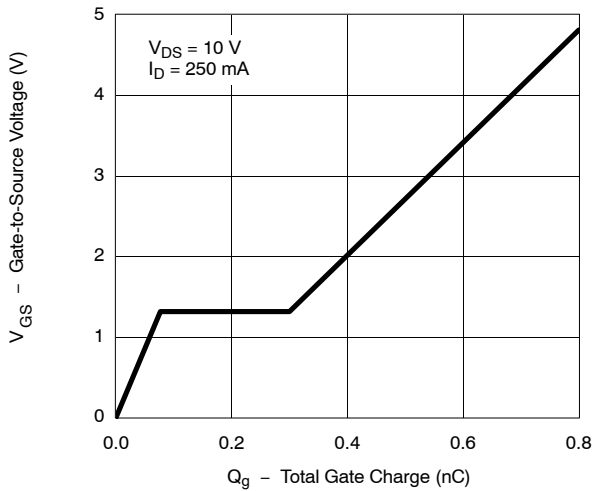
On-Resistance vs. Drain Current



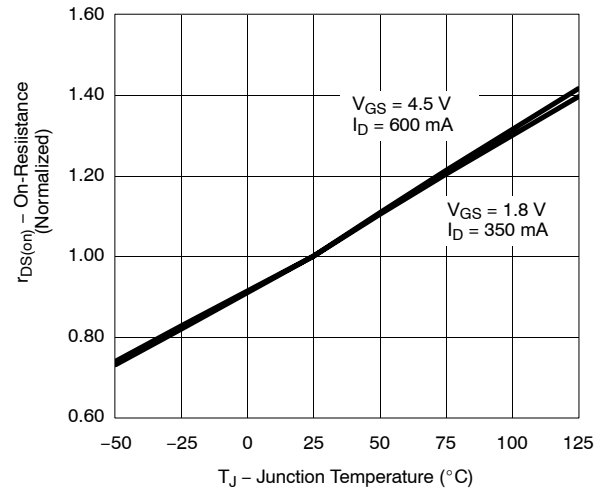
Capacitance



Gate Charge

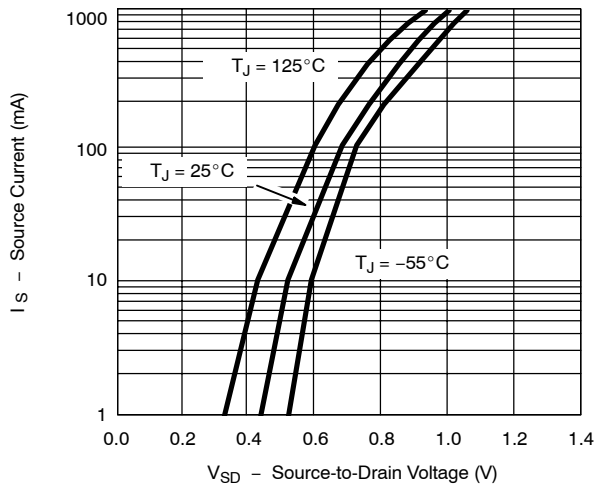


On-Resistance vs. Junction Temperature

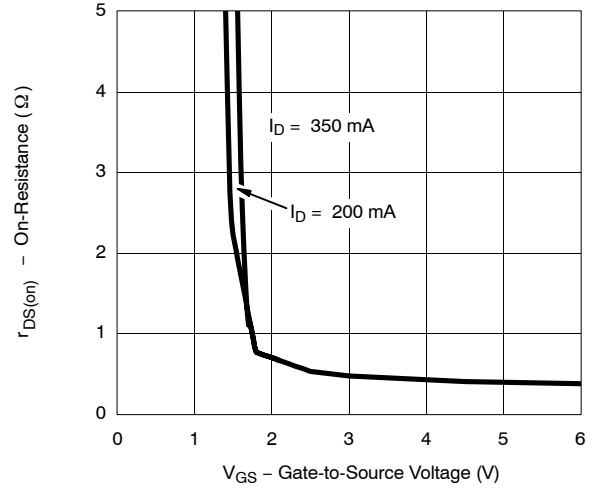


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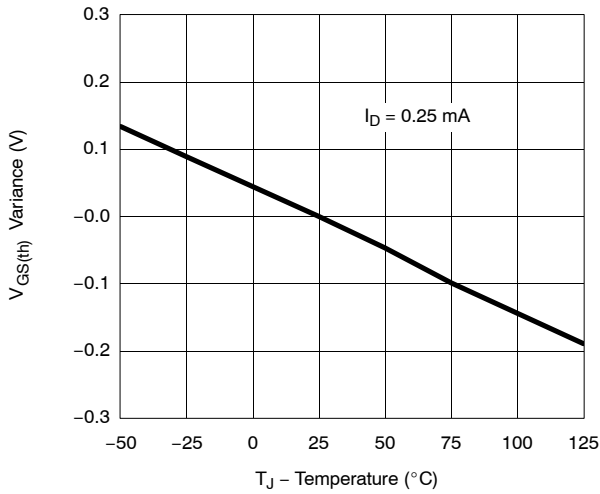
Source-Drain Diode Forward Voltage



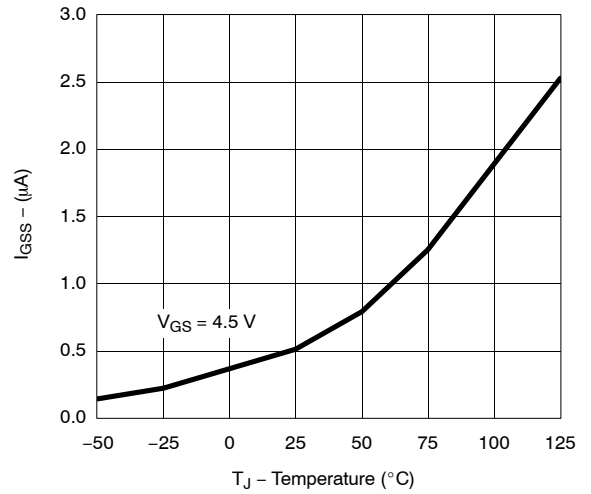
On-Resistance vs. Gate-to-Source Voltage



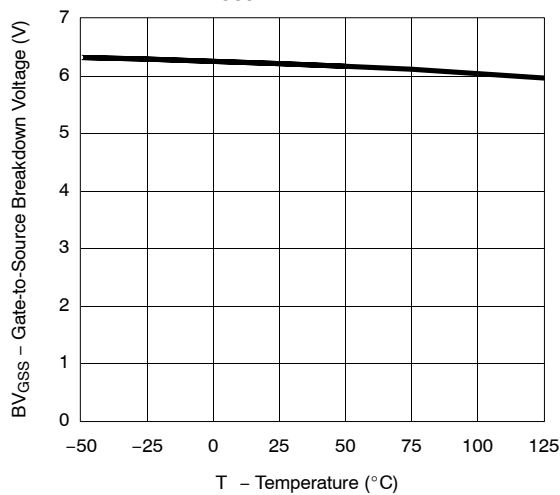
Threshold Voltage Variance vs. Temperature



IGSS vs. Temperature

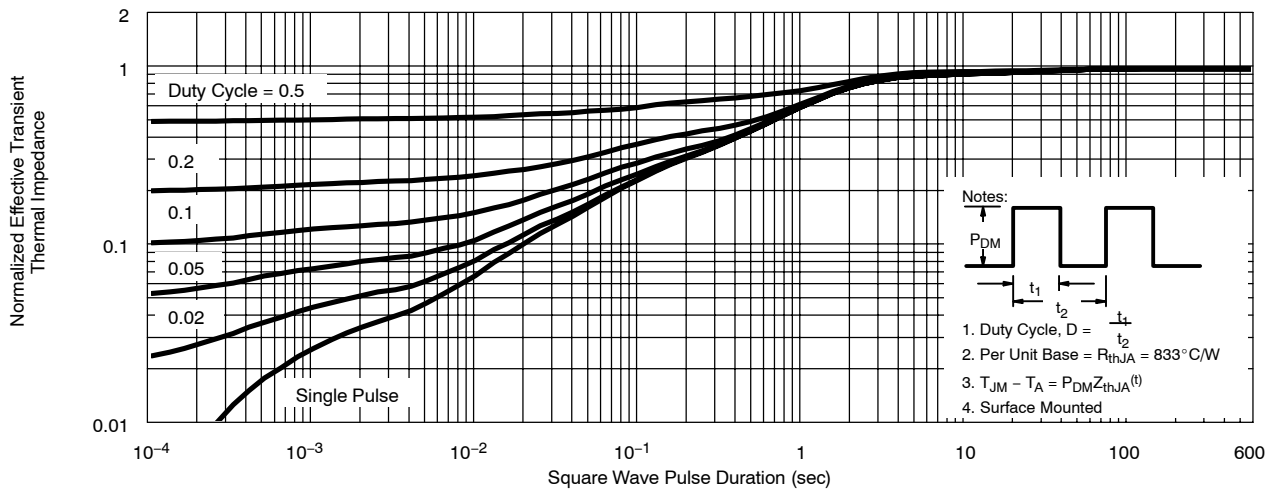


BVGSS vs. Temperature

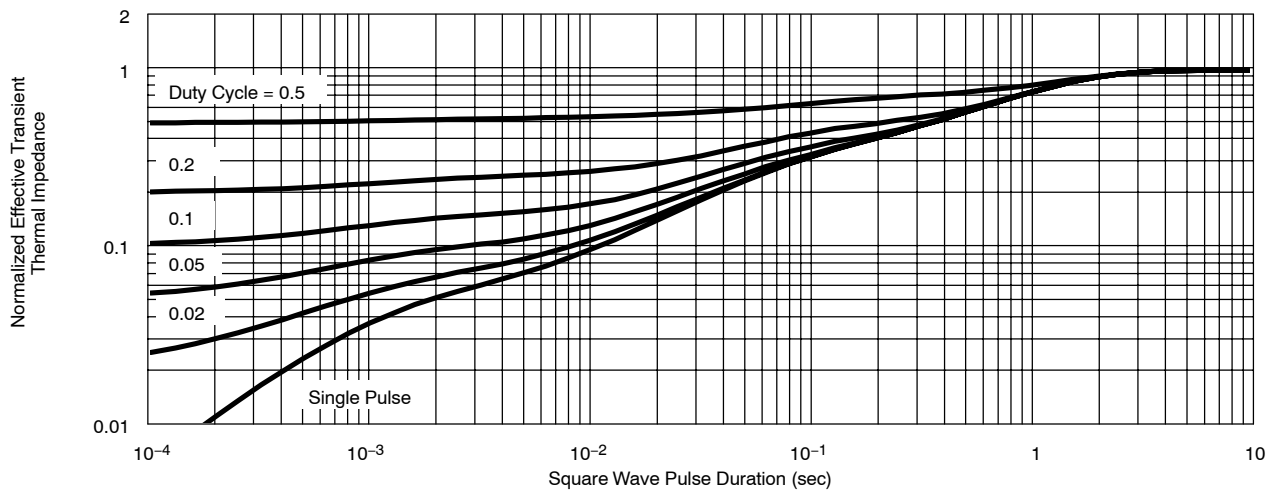


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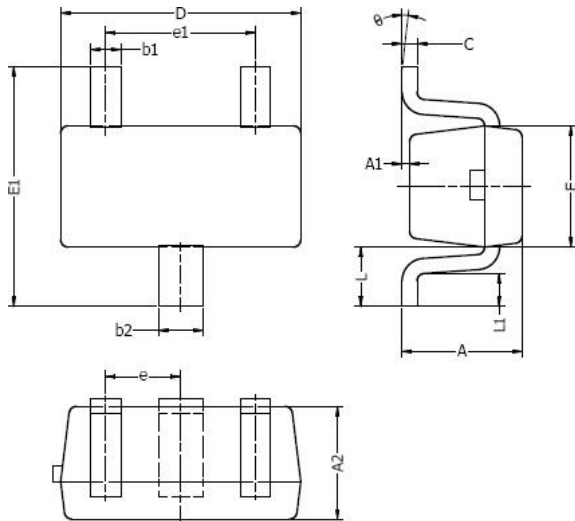
Normalized Thermal Transient Impedance, Junction-to-Ambient (SC-75A)



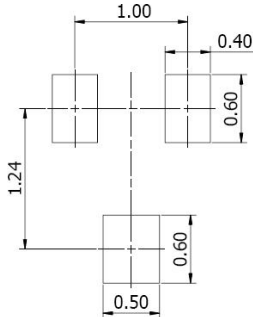
Normalized Thermal Transient Impedance, Junction-to-Foot



SOT-523 PACKAGE OUTLINE & DIMENSIONS



Typical Soldering Pattern:



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
A1	0.00	0.10	0.000	0.004
A2	0.70	0.80	0.028	0.031
b1	0.15	0.25	0.006	0.010
b2	0.25	0.35	0.010	0.014
c	0.10	0.20	0.004	0.008
D	1.50	1.70	0.059	0.067
E	0.70	0.90	0.028	0.035
E1	1.45	1.75	0.057	0.069
e	0.50 TYP.		0.020 TYP.	
e1	0.90	1.10	0.035	0.043
L	0.40 REF.		0.016 REF.	
L1	0.10	0.30	0.004	0.012
θ	0°	8°	0°	8°

NOTES:

1. Above package outline conforms to JEITA EAIJ ED-7500A SC-75A.
2. Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.