Leiditech

LM4902

N-Channel Super Trench Power MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	40V
I_D (at V_{GS}=10V)	200A
$R_{DS(ON)}$ (at V_{GS}=10V)	2.5mΩ(Max)

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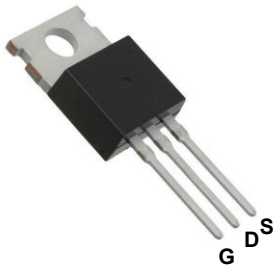

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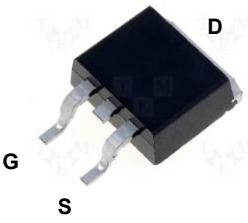

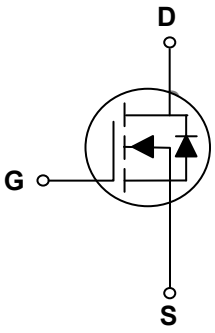

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	TC=25°C	I_D	200	A
	TC=100°C	I_D	126	A
Maximum Power Dissipation		P_D	184	W
Single pulse avalanche energy		E_{AS}	390	mJ
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		1.1	℃ /W
Thermal Resistance unction-to-Ambient	$R_{\theta JA}$		62	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On-State esistance	V_{GS}=10V, I_D=30A		1.8	2.5	mΩ
		V_{GS}=4.5V, I_D=15A		2.0	3.0	mΩ
DYNAMIC PARAMETERS						
C_{lss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		8000		pF
C_{oss}	Output Capacitance			550		pF
C_{rss}	Reverse Transfer Capacitance			420		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=20V,I_D=10A, V_{GS}=10V, R_G=10Ω		24		nS
t_r	Turn-on Rise Time			62		nS
$t_{d(off)}$	Turn-Off Delay Time			220		nS
t_f	Turn-Off Fall Time			160		nS
Q_g	Total Gate Charge	V_{DS}=20V,I_D=10A, V_{GS}=4.5V		70		nC
Q_{gs}	Gate-Source Charge			15		nC
Q_{gd}	Gate-Drain Charge			40		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=1A		0.72	1.3	V
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz		1.2		Ω

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=30V,L=0.1mH,IAS=85A., Starting TJ=25℃
3. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
4. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

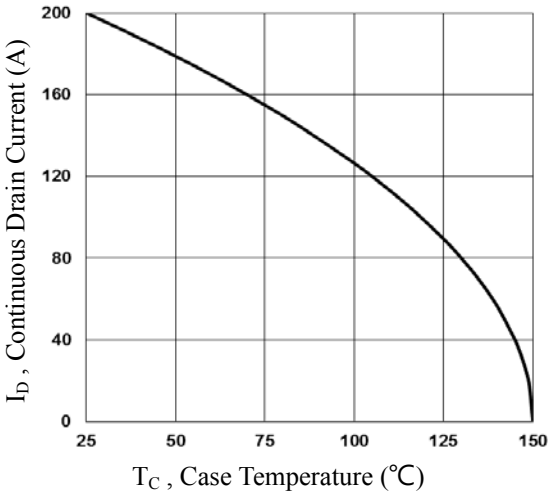

Fig.1 Continuous Drain Current vs. T_C

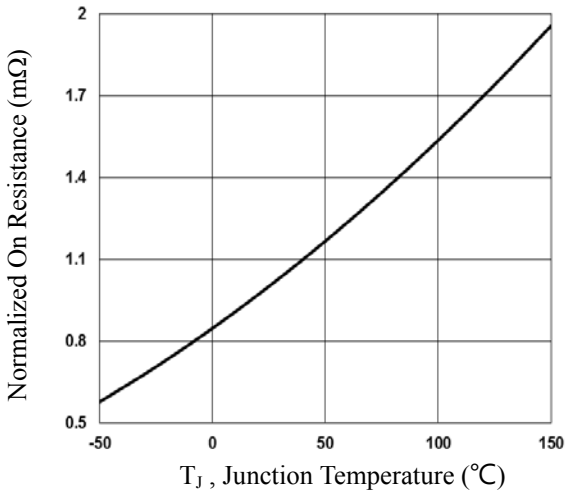

Fig.2 Normalized RDSON vs. T_J

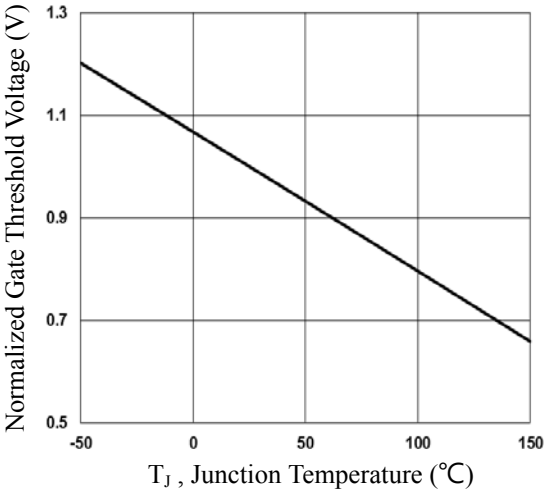

Fig.3 Normalized V_{th} vs. T_J

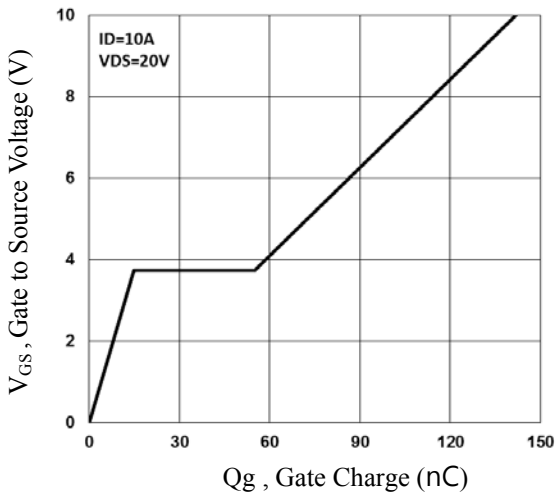

Fig.4 Gate Charge Waveform

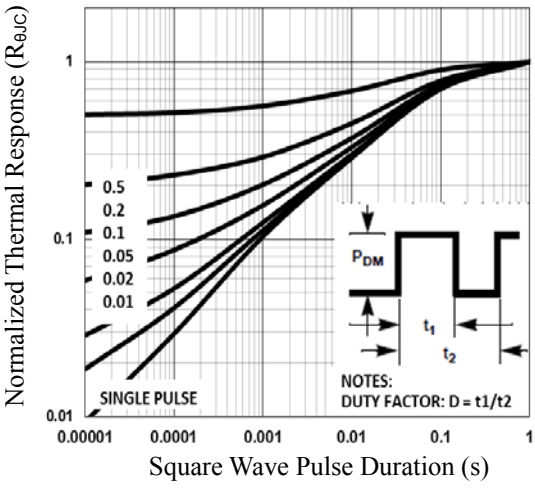

Fig.5 Normalized Transient Impedance

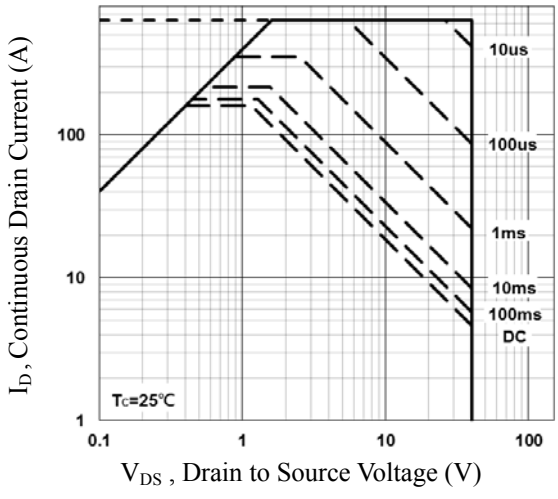

Fig.6 Maximum Safe Operation Area

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

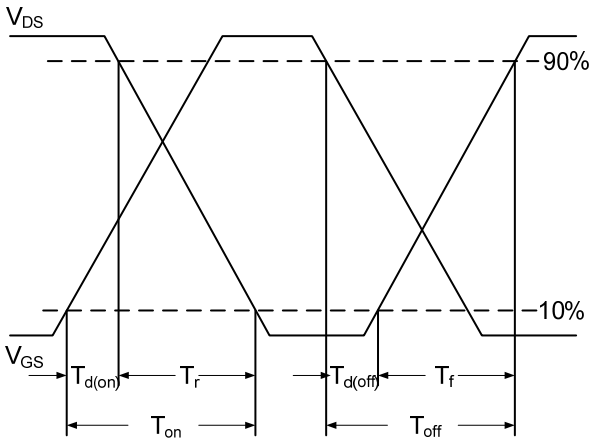

Fig.7 Switching Time Waveform

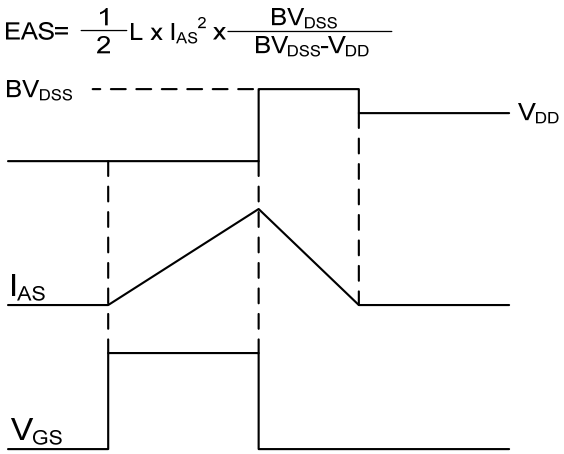

Fig.8 EAS Waveform

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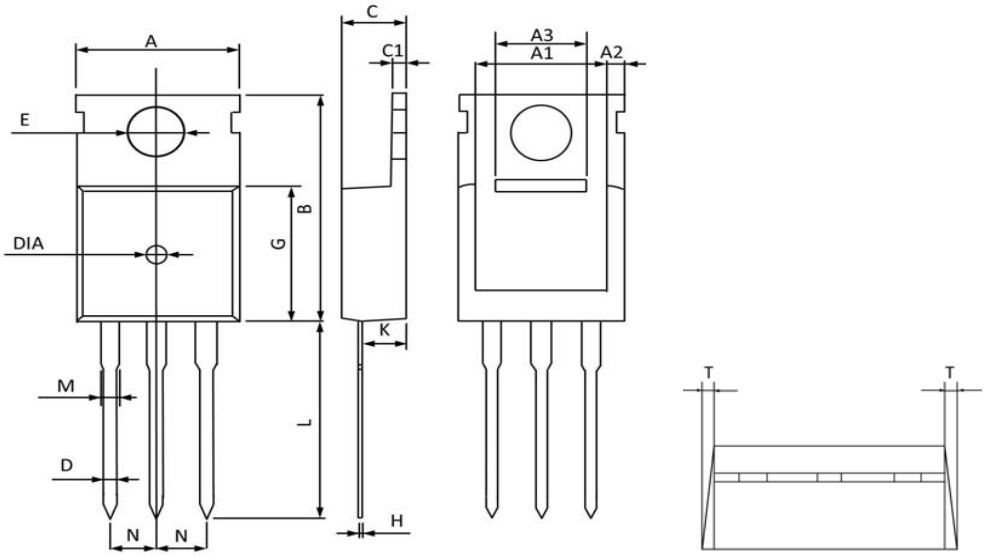

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	10.300	9.700	0.406	0.382
A1	8.840	8.440	0.348	0.332
A2	1.250	1.050	0.049	0.041
A3	5.300	5.100	0.209	0.201
B	16.200	15.400	0.638	0.606
C	4.680	4.280	0.184	0.169
C1	1.500	1.100	0.059	0.043
D	1.000	0.600	0.039	0.024
E	3.800	3.400	0.150	0.134
G	9.300	8.700	0.366	0.343
H	0.600	0.400	0.024	0.016
K	2.700	2.100	0.106	0.083
L	13.600	12.800	0.535	0.504
M	1.500	1.100	0.059	0.043
N	2.590	2.490	0.102	0.098
T	W0.35		W0.014	
DIA	Φ1.5 TYP.	deep0.2 TYP.	Φ0.059 TYP.	deep0.008 TYP.

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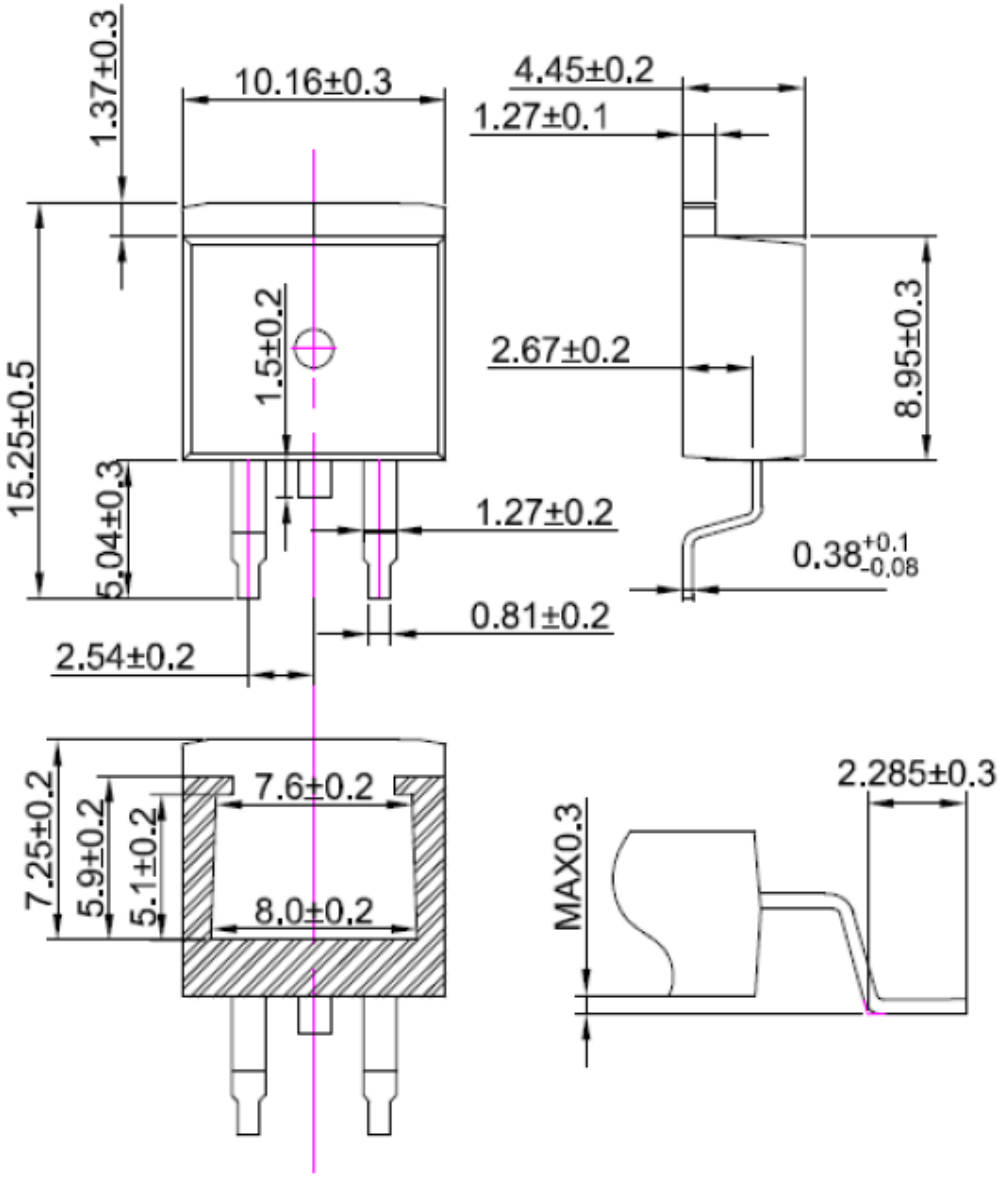

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