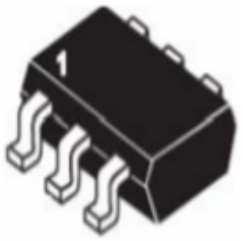
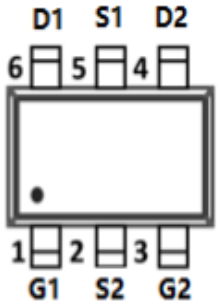
Leiditech

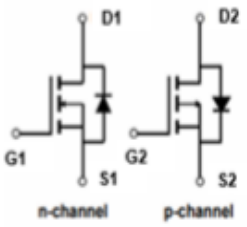
LMSC05N02A

N and P-Channel Enhancement Mode Power MOSFET





SOT-23-6



Product Summary

NMOS

- V_{DS} 20V
- I_D 5.6A
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜25 mohm
- $R_{DS(ON)}$(at V_{GS}=2.5V) ＜32 mohm
- $R_{DS(ON)}$(at V_{GS}=1.8V) ＜49 mohm

PMOS

- V_{DS} -20V
- I_D -3.7A
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜64 mohm
- $R_{DS(ON)}$(at V_{GS}=-2.5V) ＜80 mohm
- $R_{DS(ON)}$(at V_{GS}=-1.8V) ＜110 mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Wireless charger
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		V_{DS}	20	-20	V
Gate-source Voltage		V_{GS}	±10	±10	V
Drain Current	T_A=25℃ @ Steady State	I_D	5.6	-3.7	A
	T_A=70℃ @ Steady State		4.5	-3.0	
Pulsed Drain Current [A]		I_{DM}	19	-15	A
Total Power Dissipation @ T_A=25℃		P_D	1.3	1.3	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]		$R_{\theta JA}$	96	96	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
LMSC05N02A	F2	C205	3000	30000	120000	7“ reel

■ N-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V,T_C=25℃			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 4.5V, I_D=4.5A		19.5	25	mΩ
		V_{GS}= 2.5V, I_D=3.0A		25	32	
		V_{GS}= 1.8V, I_D=2.0A		33	49	
Diode Forward Voltage	V_{SD}	I_S=5.6A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				5.6	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		620		pF
Output Capacitance	C_{oss}			114		
Reverse Transfer Capacitance	C_{rss}			64		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=4.5V,V_{DS}=10V,I_D=5.6A		7.1		nC
Gate Source Charge	Q_{gs}			1.4		
Gate Drain Charge	Q_{gd}			1.9		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V,V_{DD}=10V, R_L=1.5Ω, R_{GEN}=3Ω		13		ns
Turn-on Rise Time	t_r			54		
Turn-off Delay Time	$t_{D(off)}$			18		
Turn-off Fall Time	t_f			11		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ P-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -4.5V, I_D=-3.5A		49	64	mΩ
		V_{GS}= -2.5V, I_D=-3.0A		59	80	
		V_{GS}= -1.8V, I_D=-2.0A		79	95	
Diode Forward Voltage	V_{SD}	I_S=-3.7A,V_{GS}=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-3.7	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHZ		550		pF
Output Capacitance	C_{oss}			89		
Reverse Transfer Capacitance	C_{rss}			65		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-4.5V,V_{DS}=-10V,I_D=-3.7A		4.3		nC
Gate Source Charge	Q_{gs}			0.8		
Gate Drain Charge	Q_{gd}			1.1		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V,V_{DD}=-10V, I_D=-3.7A, R_{GEN}=2.5Ω		12		ns
Turn-on Rise Time	t_r			54		
Turn-off Delay Time	$t_{D(off)}$			15		
Turn-off Fall Time	t_f			9		

C. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
D. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

N-MOS Typical Performance Characteristics

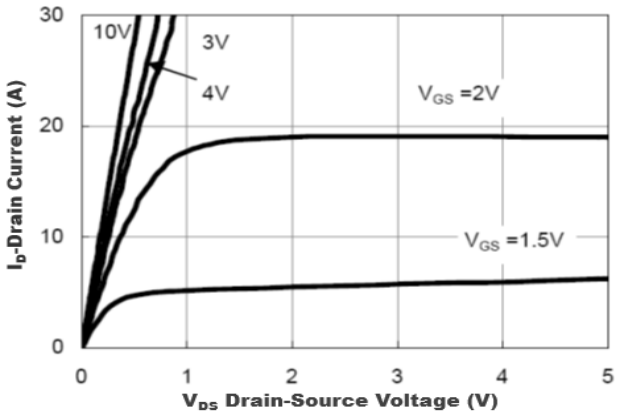


Figure1. Output Characteristics

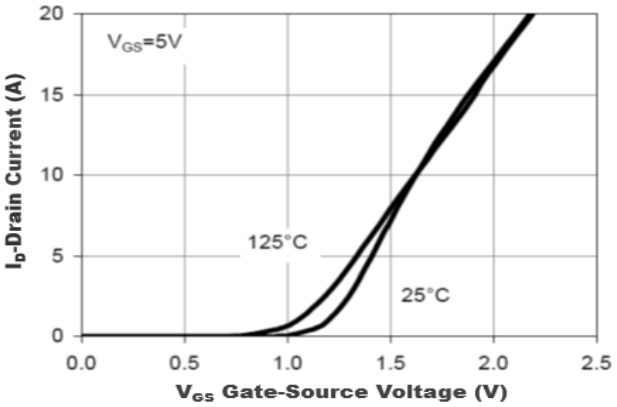


Figure2. Transfer Characteristics

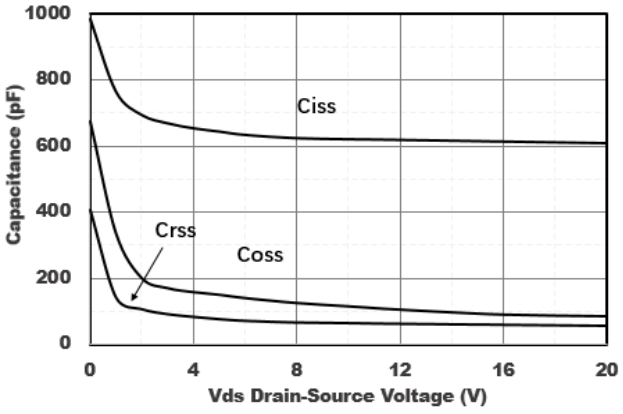


Figure3. Capacitance Characteristics

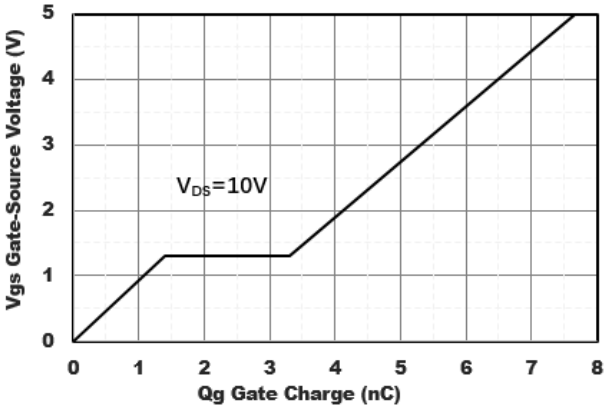


Figure4. Gate Charge

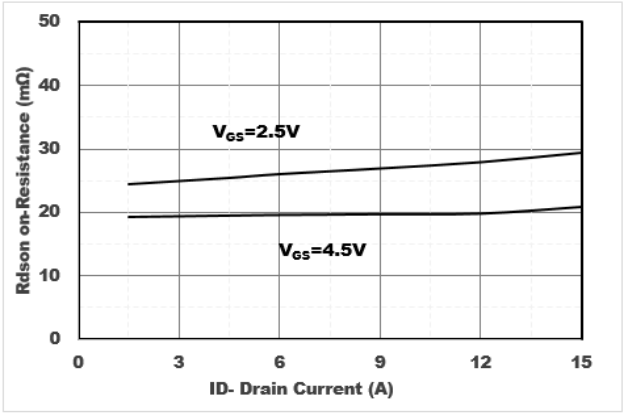


Figure5. Drain-Source on Resistance

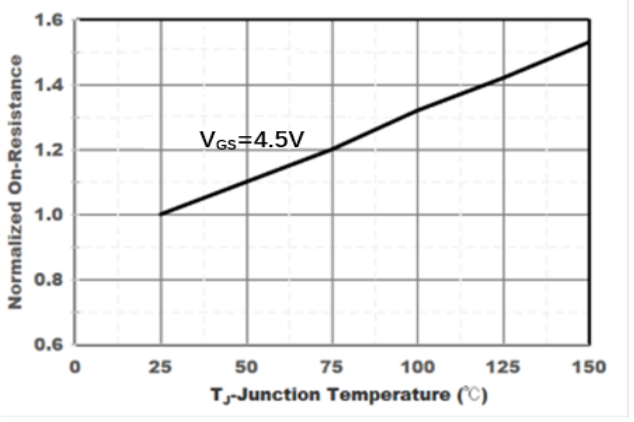


Figure6. Drain-Source on Resistance

N-MOS Typical Performance Characteristics

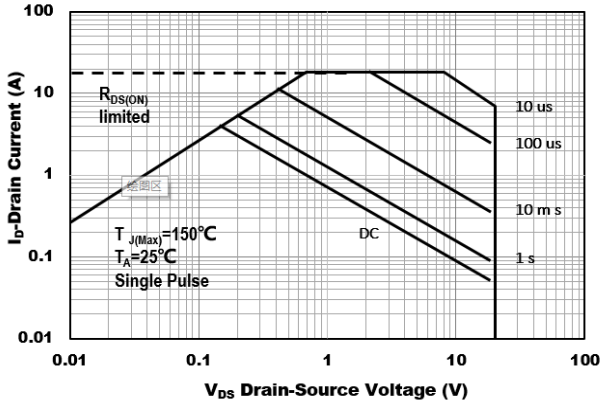


Figure7. Safe Operation Area

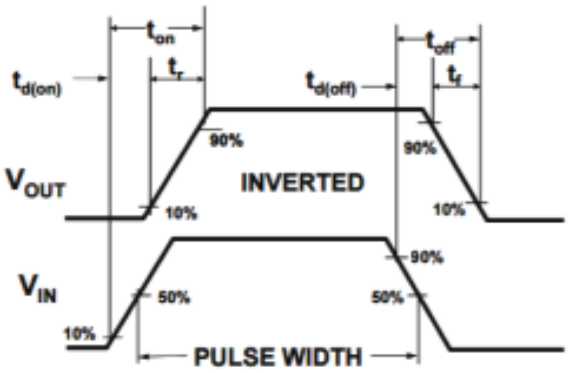


Figure8. Switching wave

P-MOS Typical Performance Characteristics

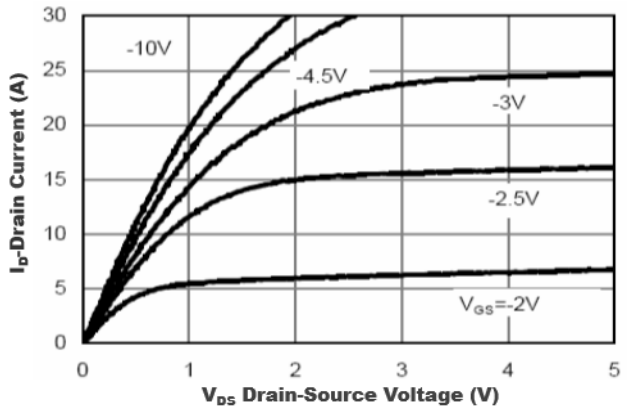


Figure1. Output Characteristics

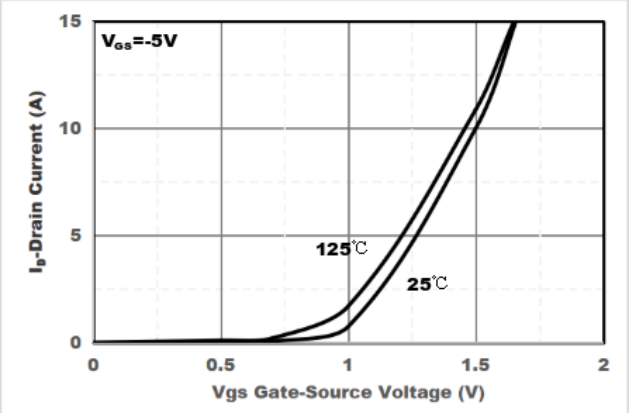


Figure2. Transfer Characteristics

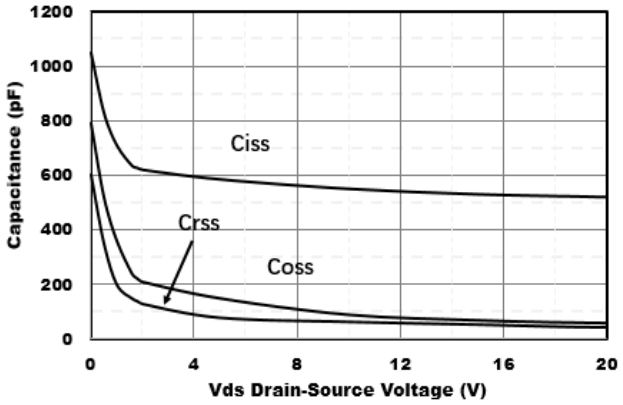


Figure3. Capacitance Characteristics

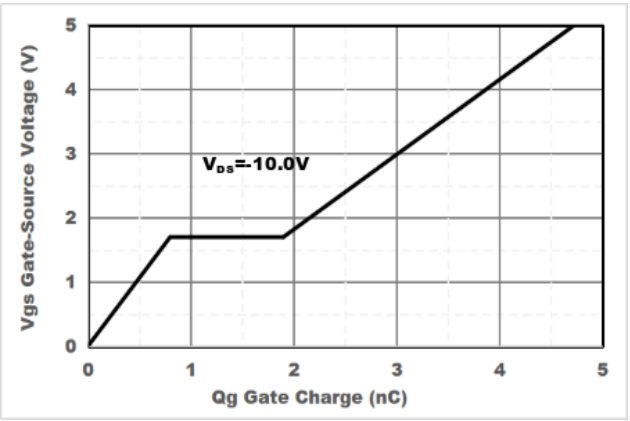


Figure4. Gate Charge

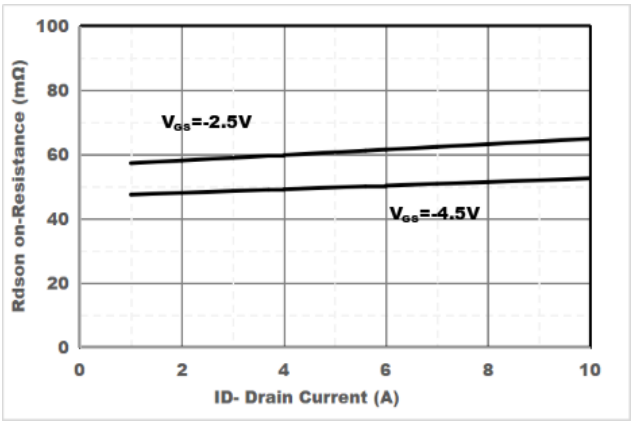


Figure5. Drain-Source on Resistance

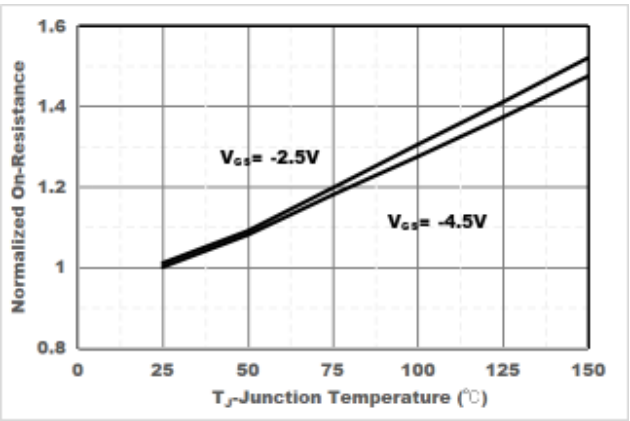


Figure6. Drain-Source on Resistance

P-MOS Typical Performance Characteristics

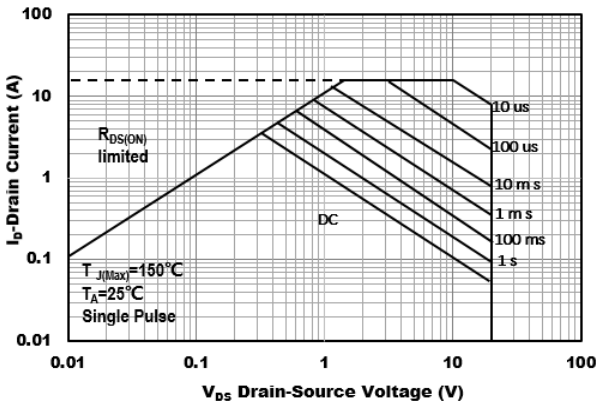


Figure7. Safe Operation Area

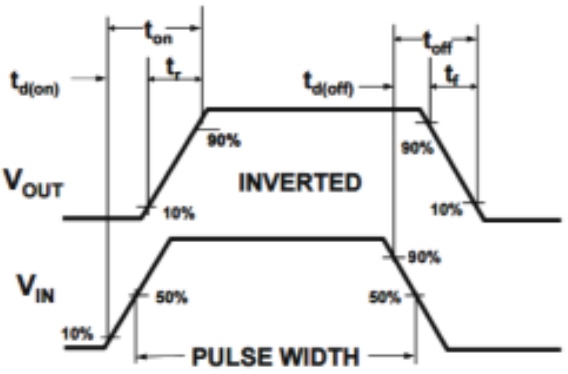
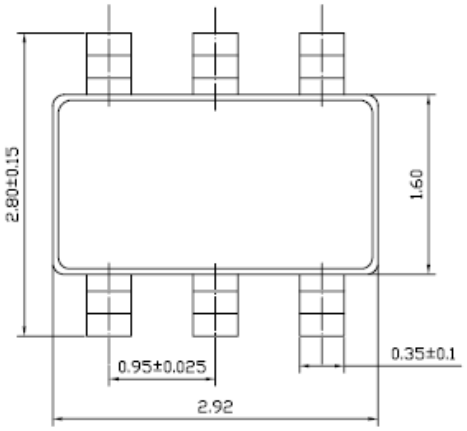
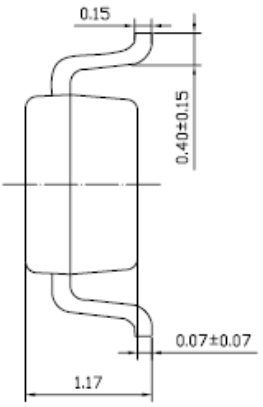


Figure8. Switching wave

■ SOT23-6 Package information





技术要求：
1.树脂体不应有崩裂、缺损等缺陷；
2.未注共差：±0.050；
3.树脂上下部X、Y方向偏差不超过0.08MAX；
4.胶体两端留废胶总和宽度不超过0.30；
5.所有单位为mm；

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