

Description

The LMAK4P50 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -500V$ $I_D = -4A$

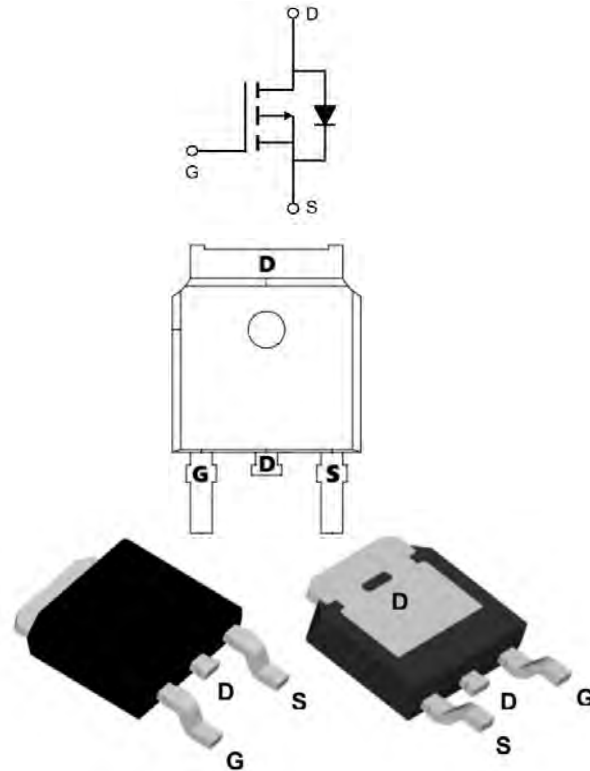
$R_{DS(ON)} < 2\Omega @ V_{GS}=10V$

Application

Brushless motor

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
LMAK4P50	TO-252	VRE25R40	2500

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-500	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-4	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-3.1	A
IDM	Pulsed Drain Current ²	-15	A
EAS	Single Pulse Avalanche Energy ³	92	mJ
IAS	Avalanche Current	4	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	80	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	110	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.5	$^\circ\text{C/W}$

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = -1\text{ mA}$	-	- 0.41	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -500\text{ V}, V_{GS} = 0\text{ V}$	-	-	- 100	μA
		$V_{DS} = -400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$ $I_D = -3.1\text{ A}^b$	-	2	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}, I_D = -3.1\text{ A}$	0.91	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = -25\text{ V},$ $f = 1.0\text{ MHz}$, see fig. 5	-	270	-	μF
Output Capacitance	C_{oss}		-	50	-	
Reverse Transfer Capacitance	C_{rss}		-	8.0	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$ $I_D = -1.1\text{ A}, V_{DS} = -320\text{ V},$ see fig. 6 and 13 ^b	-	-	13	nC
Gate-Source Charge	Q_{gs}		-	-	3.2	
Gate-Drain Charge	Q_{gd}		-	-	5.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -200\text{ V}, I_D = -1.1\text{ A},$ $R_g = 21\text{ }\Omega, R_D = 180\text{ }\Omega$, see fig. 10 ^b	-	11	-	ns
Rise Time	t_r		-	10	-	
Turn-Off Delay Time	$t_{d(off)}$		-	25	-	
Fall Time	t_f		-	24	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact ^c	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode	-	-	- 1.9	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	- 7.6	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	- 4.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = -1.1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	170	260	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	640	960	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- c. This is applied for IPAK, L_S of DPAK is measured between lead and center of die contact.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

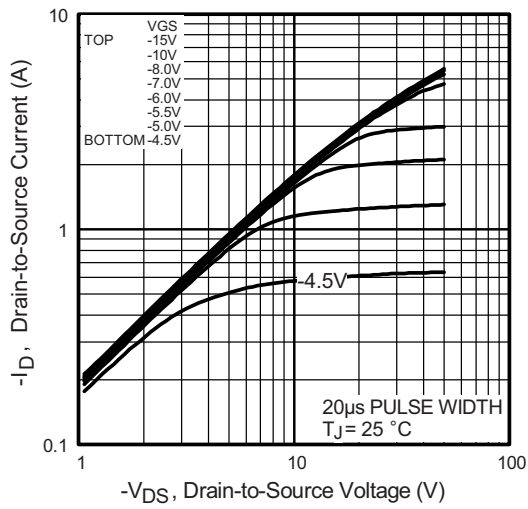


Fig. 1 - Typical Output Characteristics

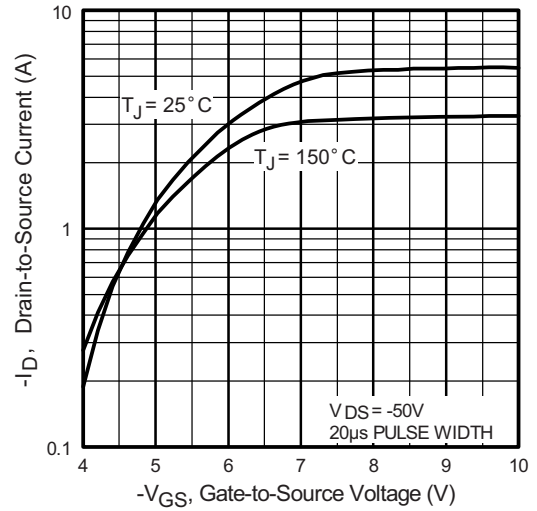


Fig. 3 - Typical Transfer Characteristics

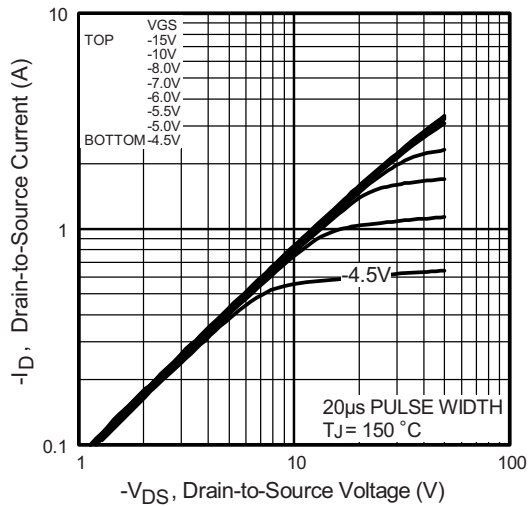


Fig. 2 - Typical Output Characteristics

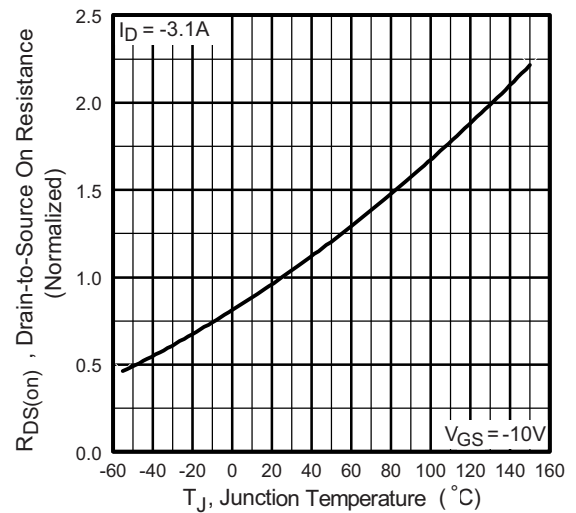


Fig. 4 - Normalized On-Resistance vs. Temperature

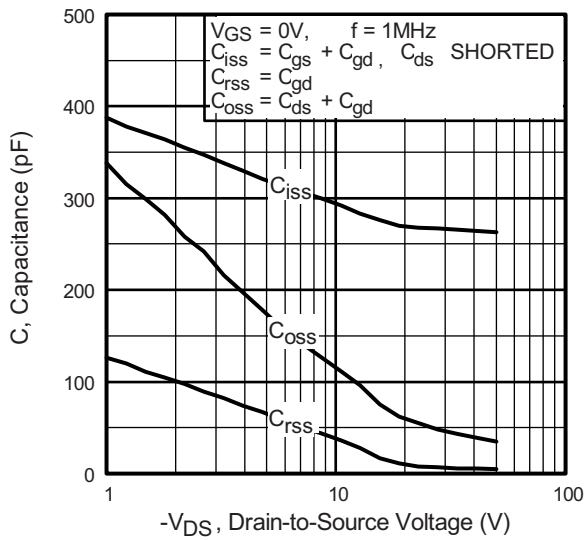


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

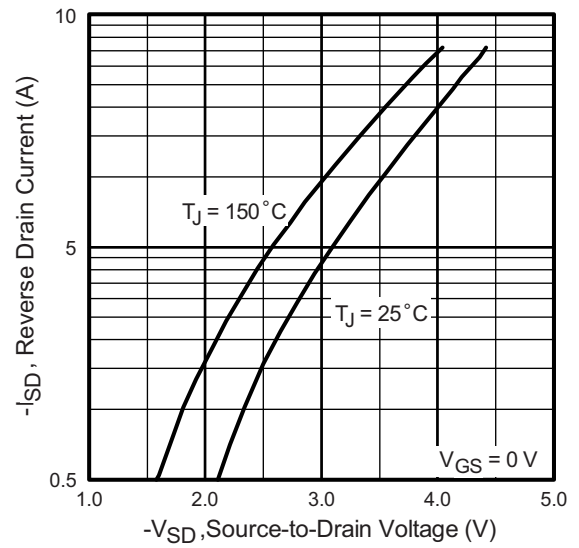


Fig. 7 - Typical Source-Drain Diode Forward Voltage

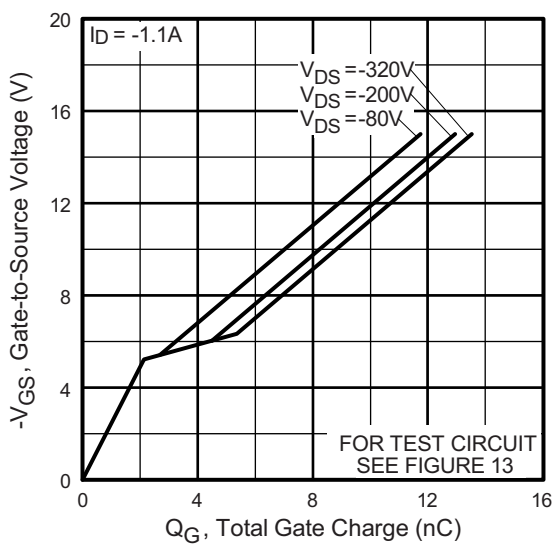


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

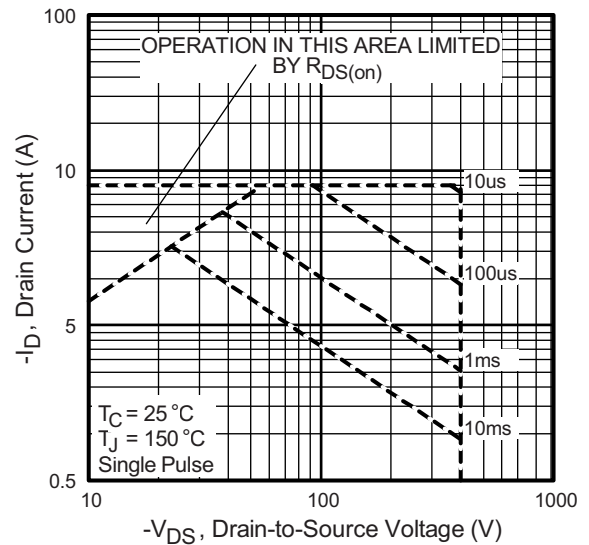


Fig. 8 - Maximum Safe Operating Area

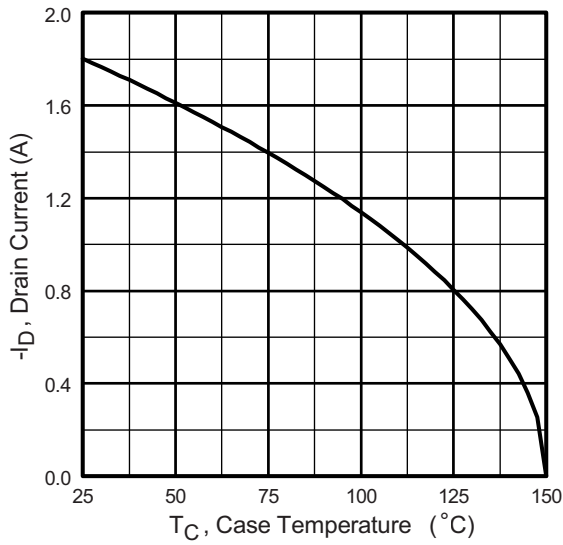


Fig. 9 - Maximum Drain Current vs. Case Temperature

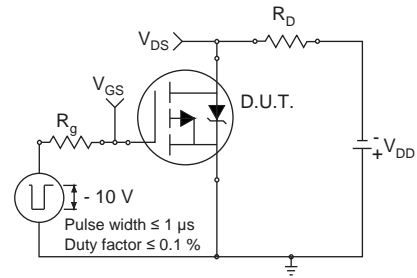


Fig. 10a - Switching Time Test Circuit

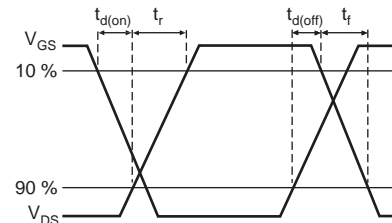


Fig. 10b - Switching Time Waveforms

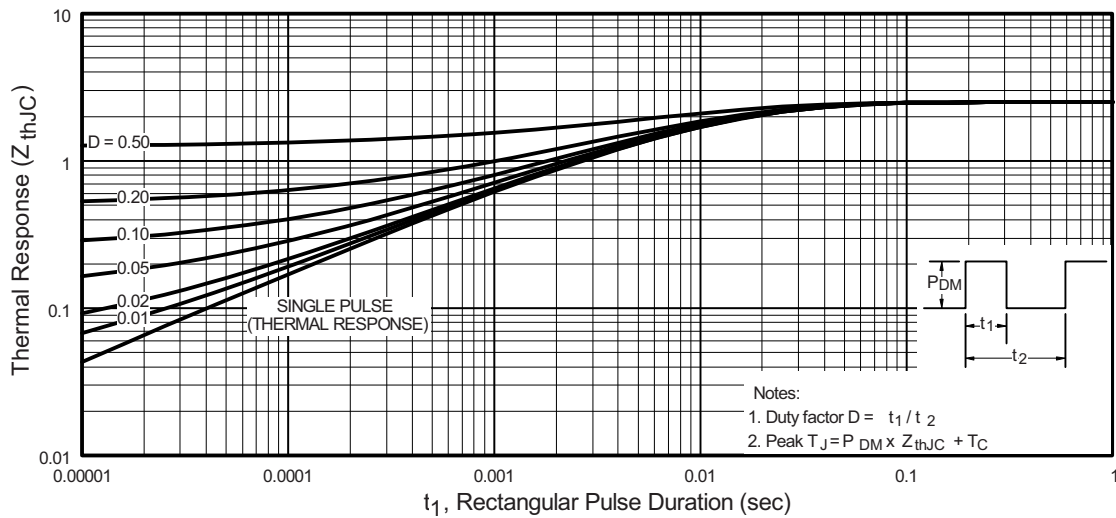
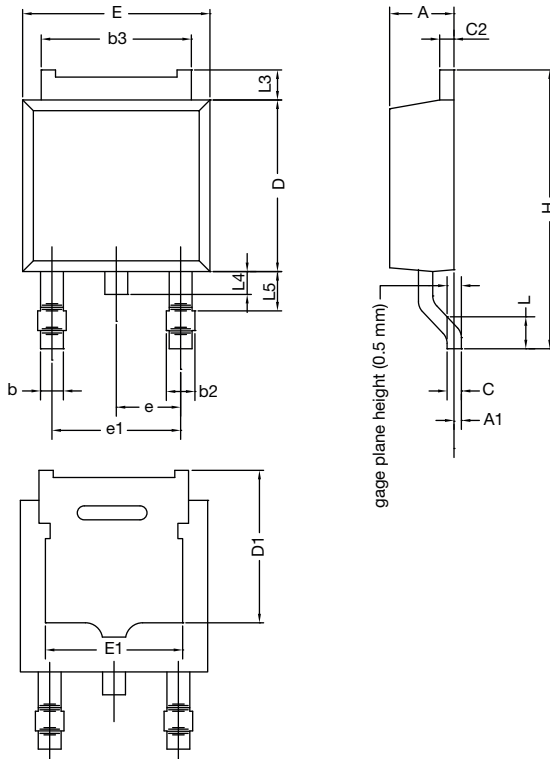


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

TO-252 Case Outline



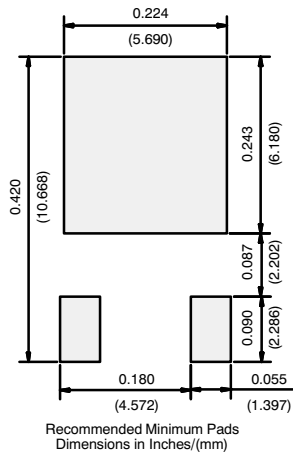
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T16-0236-Rev. P, 16-May-16
DWG: 5347

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



NOTICE

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