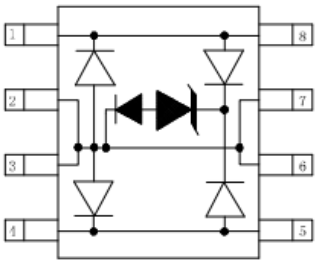
LC03-3.3

Low Capacitance 3.3V TVS

Features

- Ultra low leakage: nA level
- Operating voltage: 3.3V
- Low clamping voltage
- Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±30kV
    - Contact discharge: ±30kV
  - IEC61000-4-4 (EFT) 40A (5/50ns)
  - IEC61000-4-5 (Lightning) 100A (8/20μs)
- RoHS Compliant

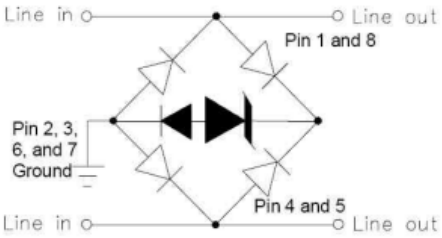
Dimensions SO-8



Applications

- T1/E1 Line Cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet
- Set Top Box
- ISDN Interfaces
- Low Voltage Interfaces

Pin Configuration



Mechanical Characteristics

- Package: SO-8
- Lead Finish: Lead Free
- UL Flammability Classification Rating 94V-0
- Quantity Per Reel:2,500 pcs
- Reel Size:7 inch
- Device Marking: LC-3.3

Absolute Maximum Ratings (Tamb=25°C unless otherwise specified)

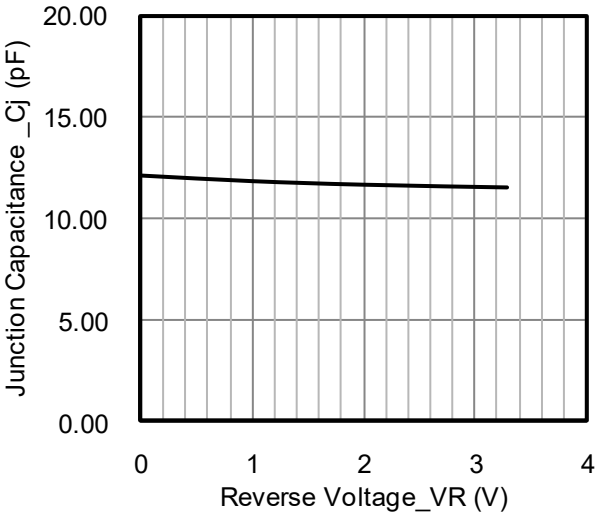
Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppp	1800	W
ESD per IEC 61000−4−2 (Air)	V_{ESD}	± 30	kV
ESD per IEC 61000−4−2 (Contact)		± 30	
Operating Temperature Range	T_J	-55 to +125	℃
Storage Temperature Range	T_{STJ}	-55 to +150	℃

Electrical Characteristics(TA=25°C unless otherwise specified)

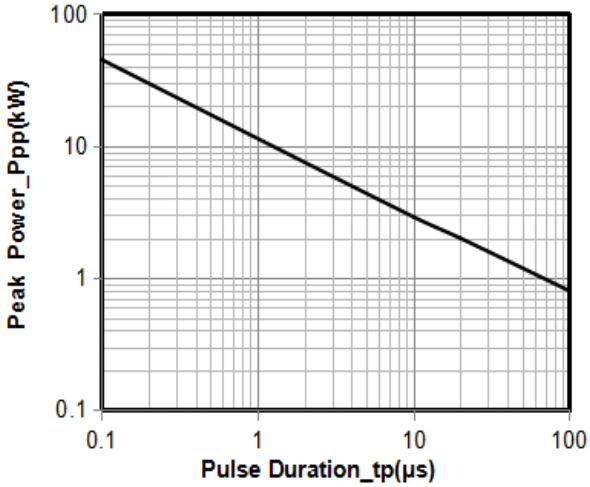
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			3.3	V	Any I/O Pin to GND
Punch-Through Voltage	V_{PT}	3.5			V	I_T = 2μA, any I/O Pin to GND
Snap-Back Voltage	V_{SB}	2.8			V	I_T = 50mA, any I/O Pin to GND
Reverse Leakage Current	I_R			1	μA	V_{RWM} = 3.3V, any I/O Pin to GND
Clamping Voltage	V_C			11	V	I_{PP} = 50A (8 x 20μs pulse), any I/O Pin to GND
Clamping Voltage	V_C			13	V	I_{PP} = 50A (8 x 20μs pulse), between I/O Pins
Clamping Voltage	V_C			15	V	I_{PP} = 100A (8 x 20μs pulse), any I/O Pin to GND
Clamping Voltage	V_C			18	V	I_{PP} = 100A (8 x 20μs pulse), between I/O Pins
Junction Capacitance	C_J		16	25	pF	VR = 0V, f = 1MHz, any I/O Pin to GND
Junction Capacitance	C_J		8	12	pF	VR = 0V, f = 1MHz, between I/O Pins

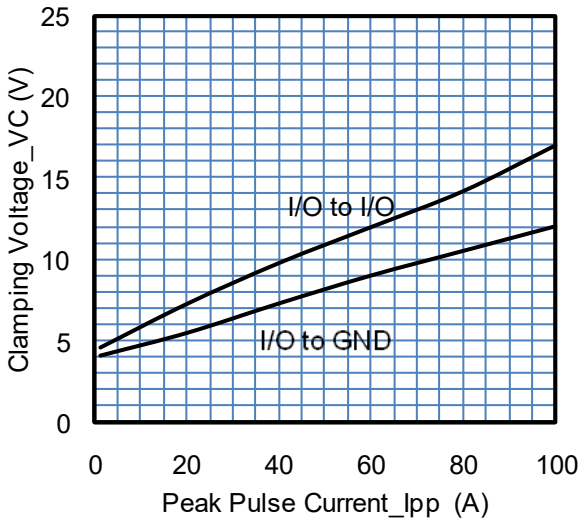
Note 1: I/O Pins are Pin 1, 4, 5 and 8

Typical Performance Characteristics(TA=25°C unless otherwise specified)

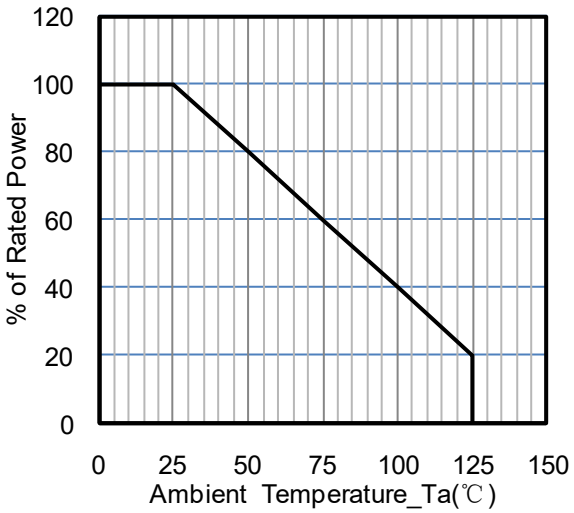


Junction Capacitance vs. Reverse Voltage

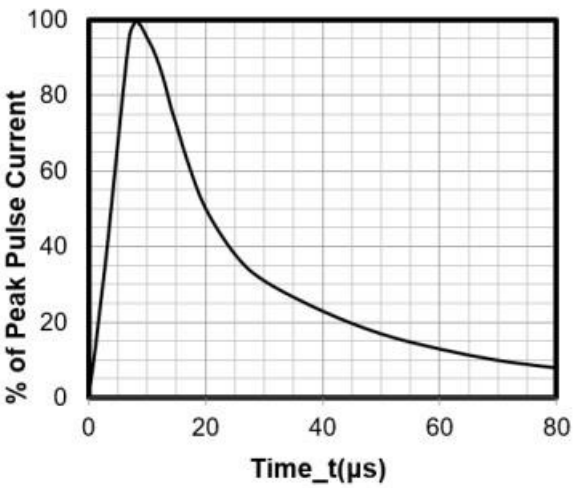




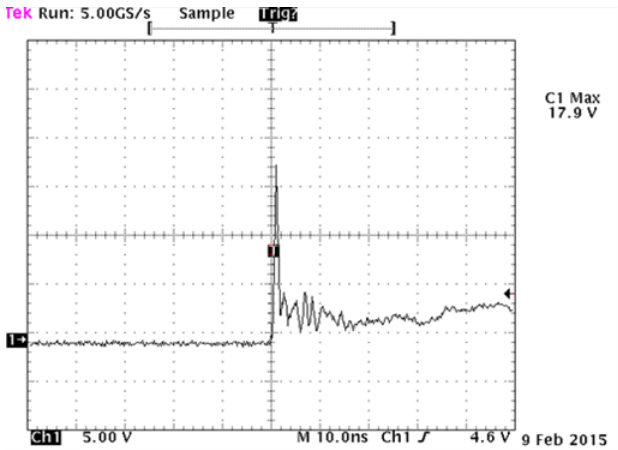
Clamping Voltage vs. Peak Pulse Current



Power Derating Curve



8 X 20μs Pulse Waveform



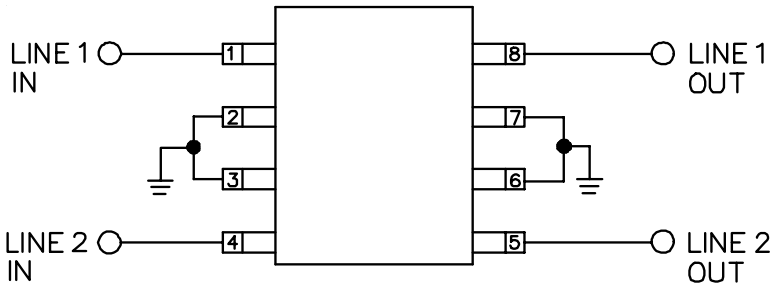
Note：Data is taken with a 10x attenuator

ESD Clamping Voltage

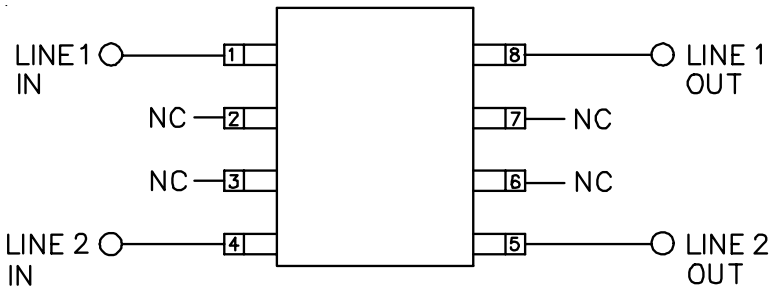
+8 kV Contact per IEC61000−4−2

Typical Application

The LC03-3.3 is designed to protect two high speed data lines (one differential pair) from transient over-voltages which result from lightning and ESD. The device can be configured to protect in differential (Line to Line) and common (Line to Ground) mode. Data line inputs/outputs are connected at pins 1 to 8, and 4 to 5 as shown below. Pins 2, 3, 6, 7 are connected to ground. These pins should be connected directly to a ground plane on the board for the best results, the path length is kept as short as possible to minimize parasitic inductance. In applications where high common voltages are present, differential protection is achieved by leaving pins 2, 3, 6, and 7 not connected.

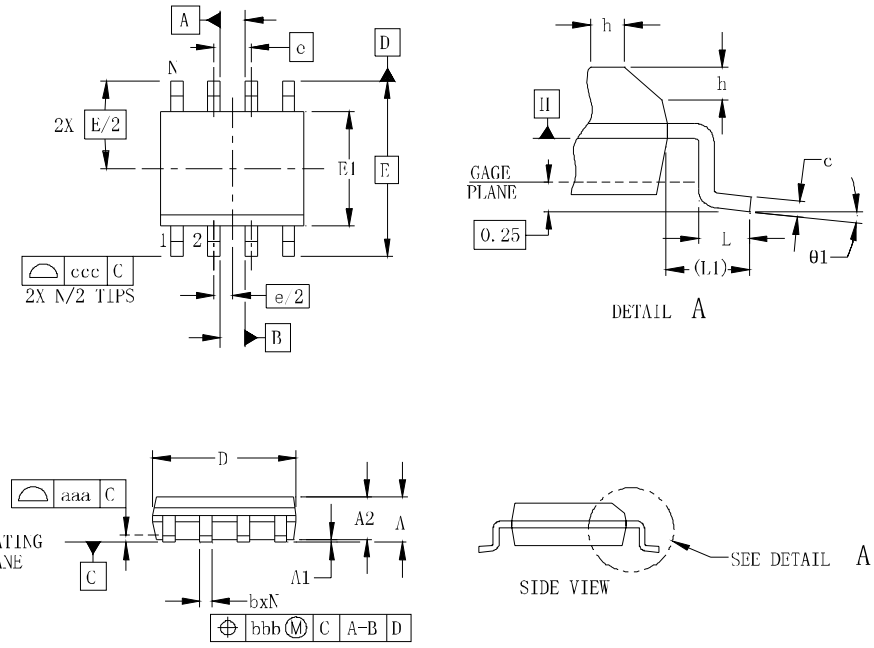


Connection for differential (Line to Line) and common mode protection (Line to Ground)



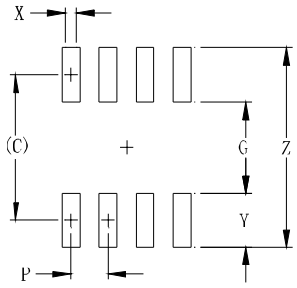
Connection for differential protection (Line to Line)

SOP-8 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.25		1.65	0.049		0.065
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.80	3.90	4.00	0.150	0.154	0.157
E	6.00 BSC			0.236 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.40	0.72	1.04	0.016	0.028	0.041
L1	(1.04)			(0.041)		
N	8			8		
θ1	0°		8°	0°		8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ccc	0.20			0.008		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	(5.20)	0.205
G	3.00	0.118
P	1.27	0.050
X	0.60	0.024
Y	2.20	0.087
Z	7.40	0.291

NOTICE

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